MINISTRY OF
ELECTRONICS &
INFORMATION TECHNOLOGY
GOVERNMENT OF INDIA

Chips to Startup Programme
An initiative by Ministry of Electronics and IT, Government of India

WEBINAR ON
OPEN SOURCE CHIP DESIGN FLOW FOR SILICON SOVEREIGNTY

Chips to Startup (C2S) Programme and Design Linked Incentive (DLI) Scheme of MeitY introduces the Efabless chipIgnite solution for creating and fabricating your own chip.

May 27, 2022
10:00 AM -11:00 AM (IST)

Speakers

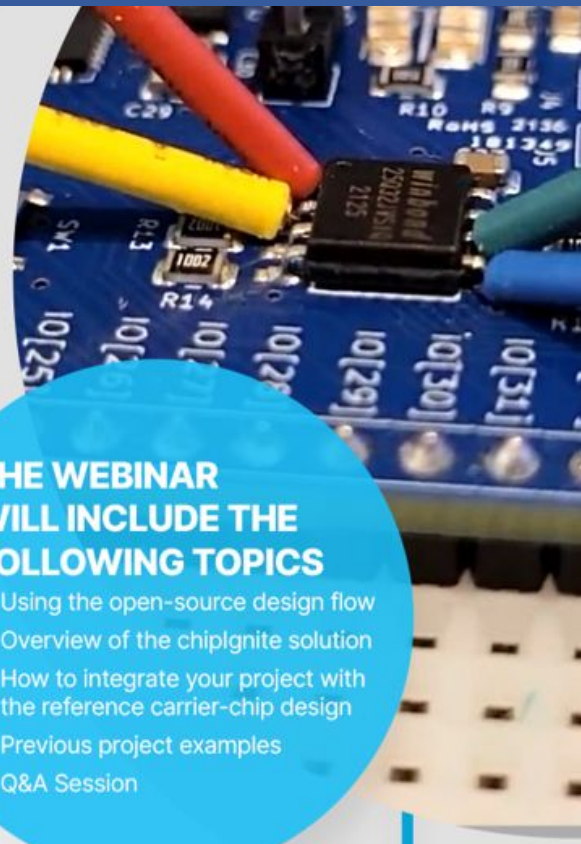
Jeff DiCorpo
SVP & General Manager, Efabless Corporation

Mohamed Kassem
Co-founder and CTO of Efabless Corporation

Scan QR Code for Registration

Registration Link

https://efabless.zoom.us/webinar/register/WN_HPRA0r7aQCeoZzaWWo0I8g



THE WEBINAR WILL INCLUDE THE FOLLOWING TOPICS

- Using the open-source design flow
- Overview of the chipIgnite solution
- How to integrate your project with the reference carrier-chip design
- Previous project examples
- Q&A Session

Why is it “hard” to design chips

Limited access to **knowledge**

Limited access **technology**

Costly **manufacturing**

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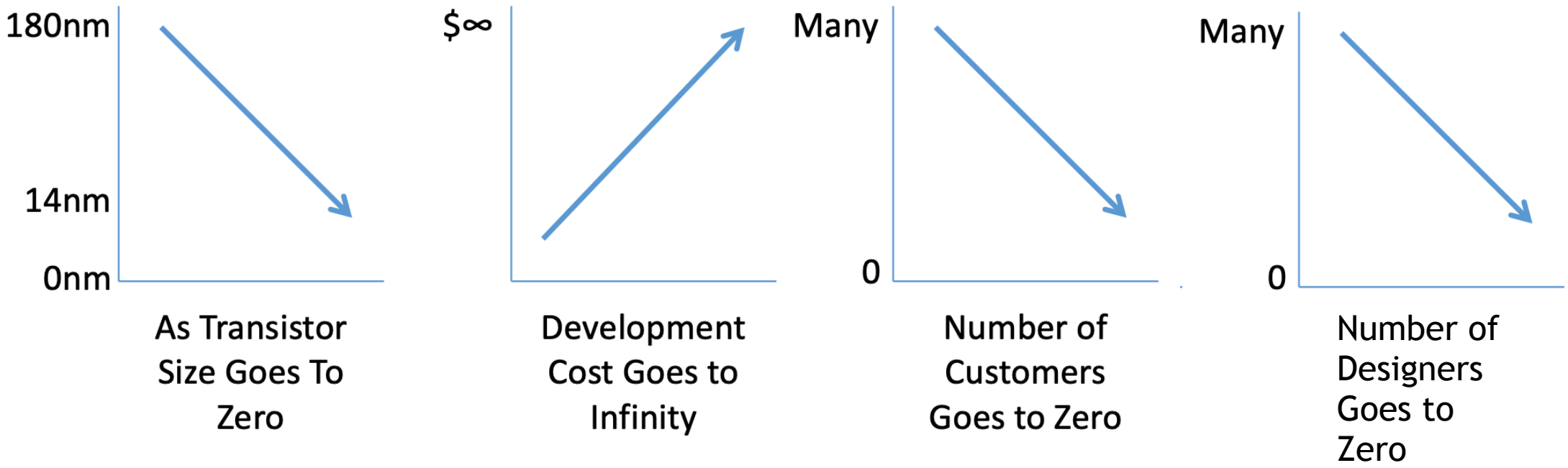
CHIP INDUSTRY TRENDS



Source: Mike Noonen

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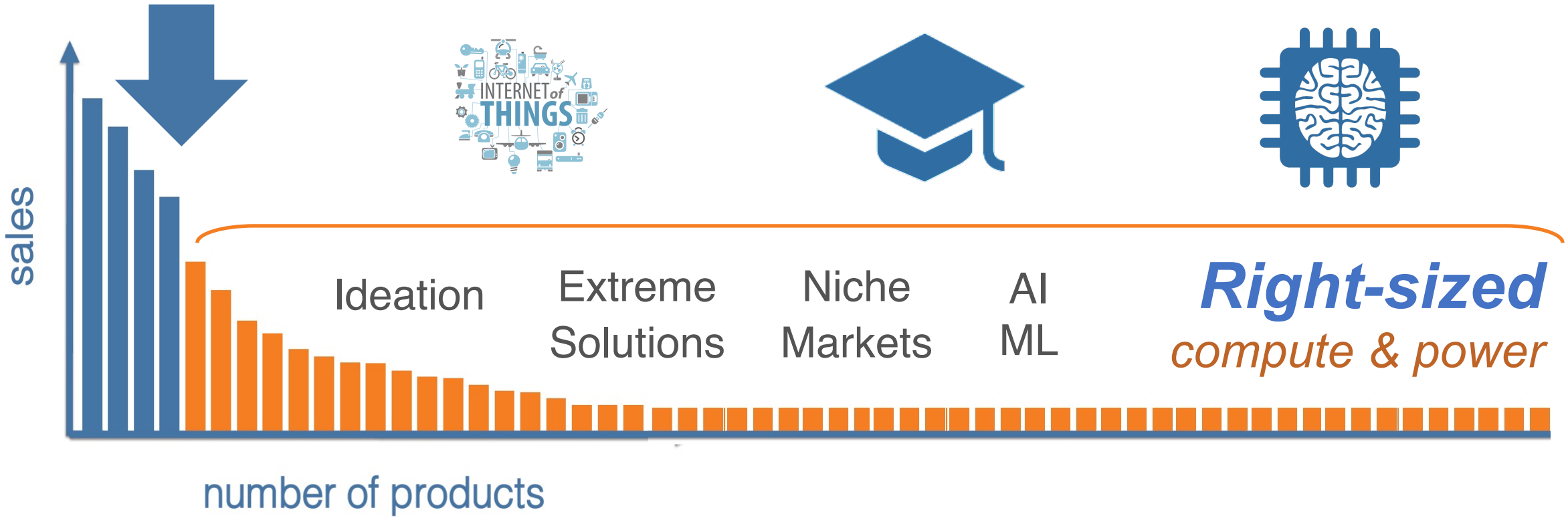
WE NEED A 1000X PRODUCT DESIGNERS

Long-tail Innovation is required on a massive scale to meet demand

10,000's of Products



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We need to

Simplify the process of **Chip creation** and open it **to Everyone**

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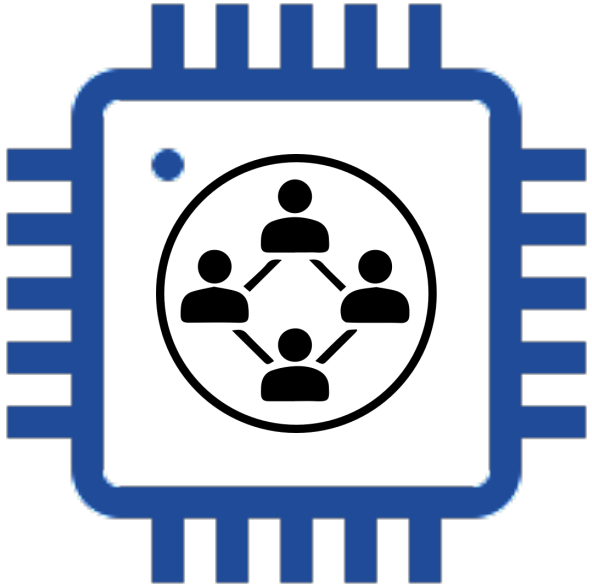
YouTube for Chips



We Make Everyone a Chip Creator

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How would we simplify chip design?

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Think what **app stores** did to software innovation.

Simplified *(democratized)*

the **development tools**

the **business process**

the **connection to customers**

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Think what **app stores** did to software innovation.

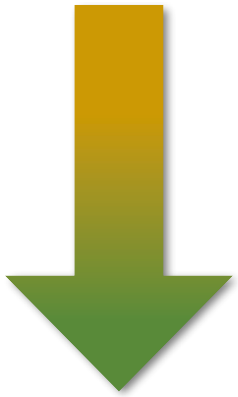
Simplified (democratized)

the **development tools**

the **business process**

the **connection to customers**

Thousands



At least

Millions

Including kids

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Think that we apply the same approach to chip design

Simplify (democratize)

the **access** to chip design tools & PDK

the **business process**

the **connection to customers**

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Think that we apply the same approach to chip design

Thousands

Simplify (democratize)

the **access** to chip **design tools** & PDK

the **business process**

the **connection to customers**

At least

Millions

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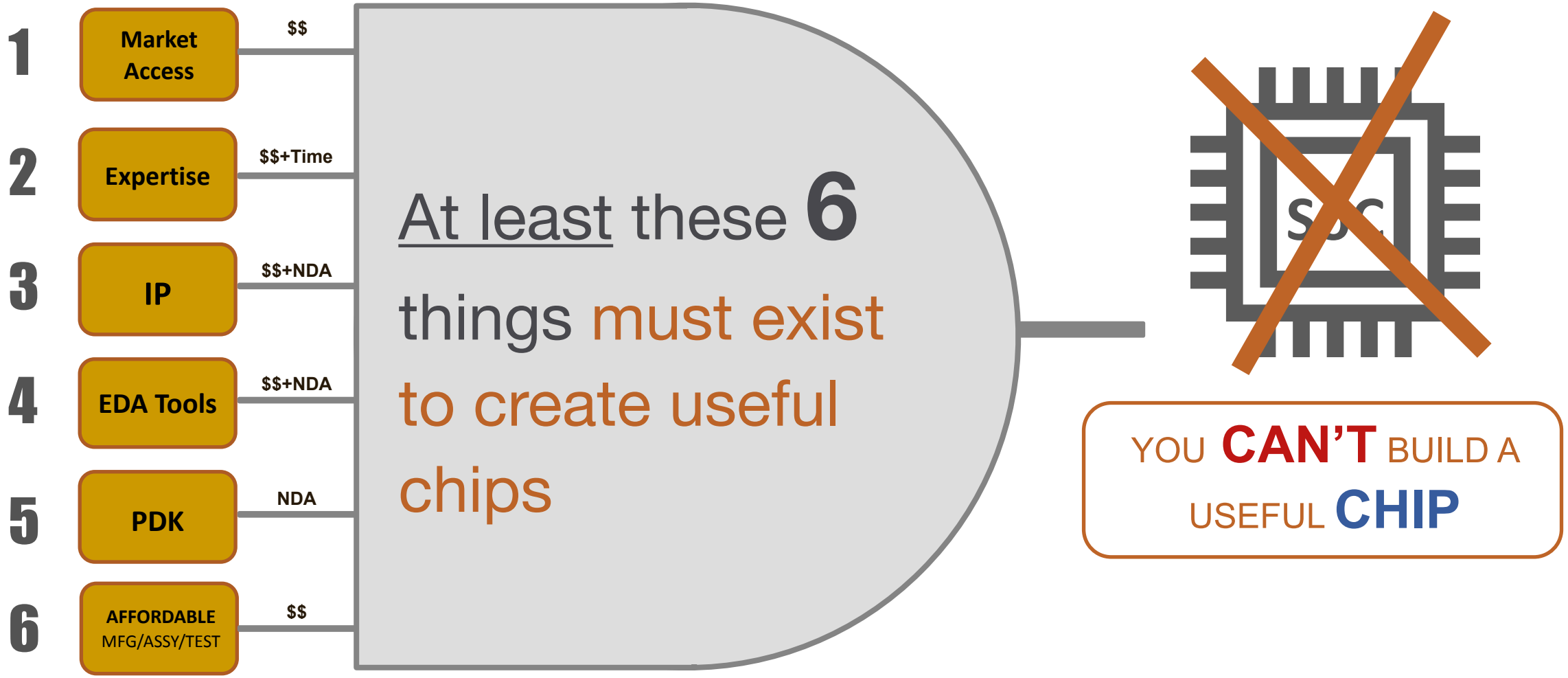
….. too complicated



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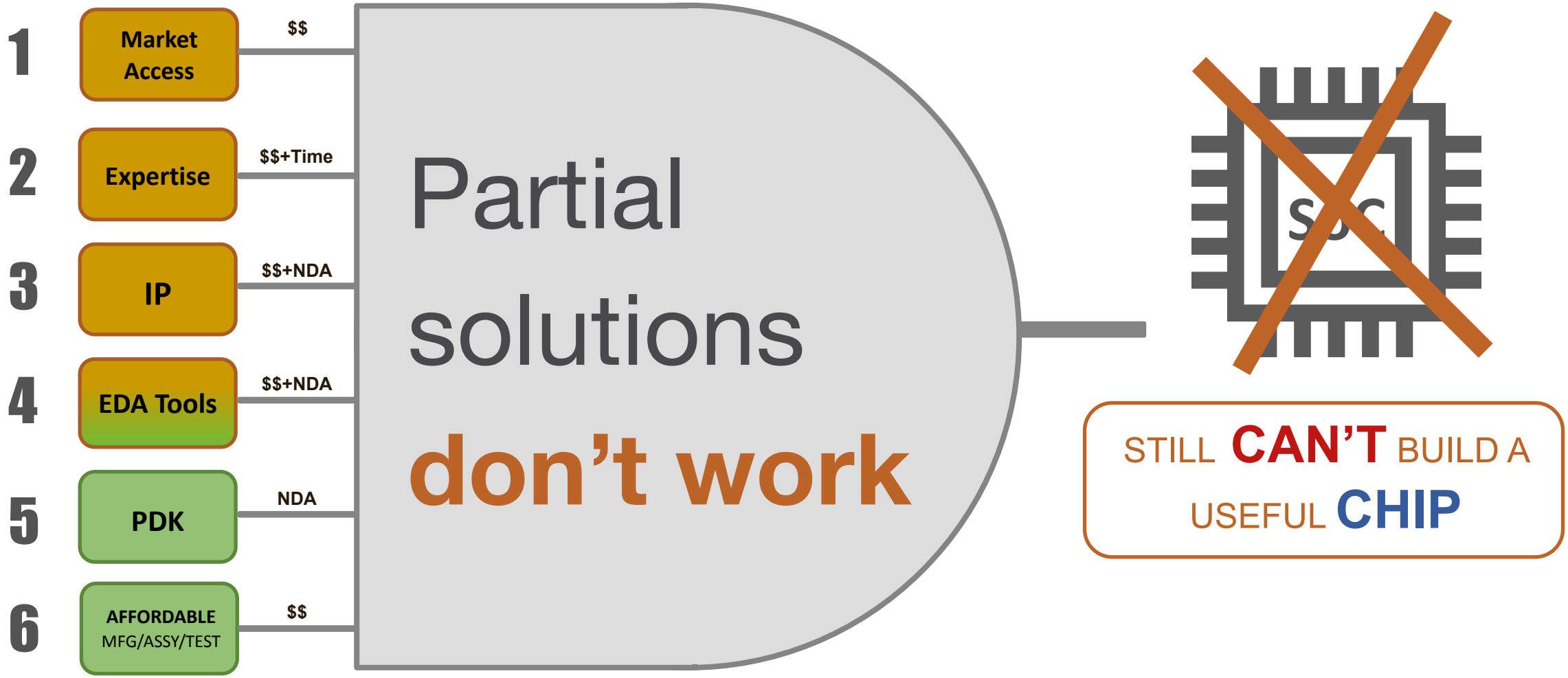
….. still too complicated



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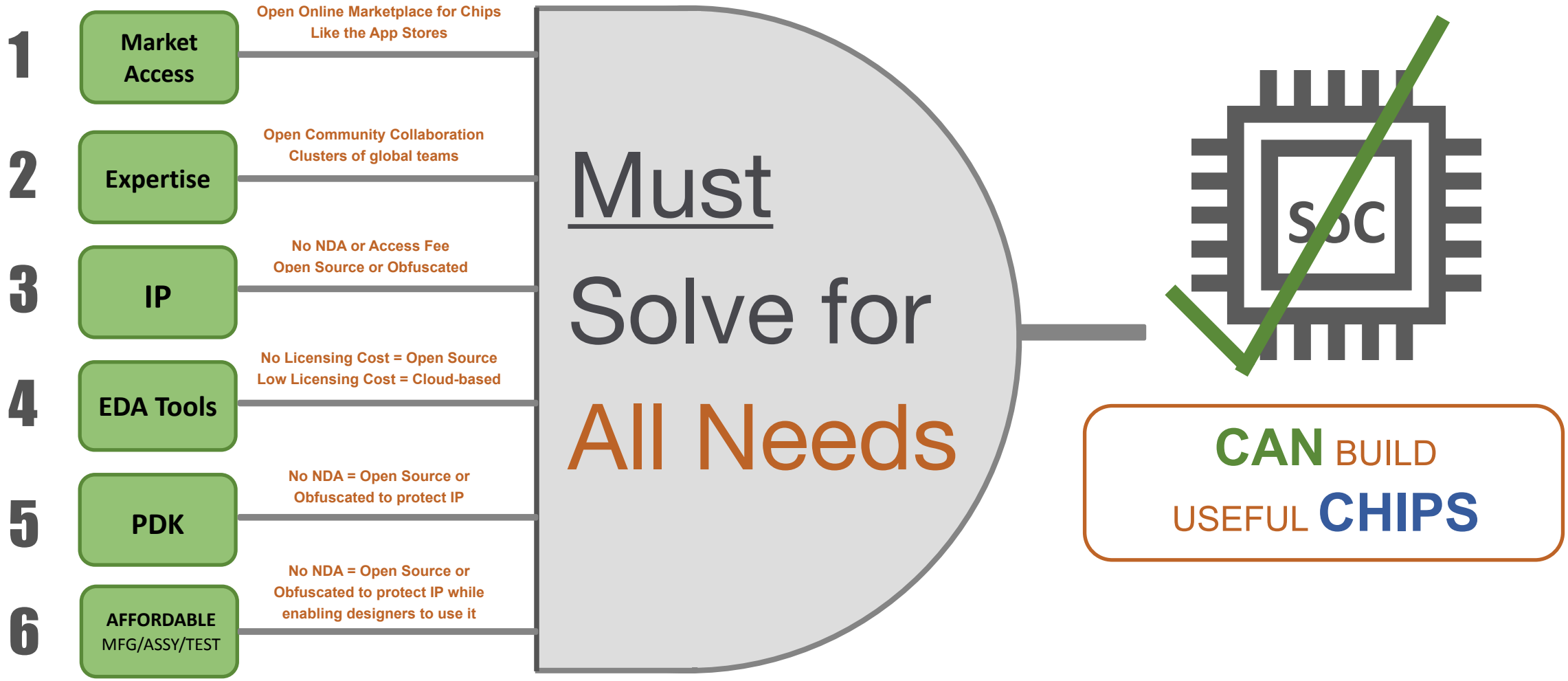
….. what we need …



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How do we simplify chip design? **#1**

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Open access to technology PDK

No NDA, nothing to sign - it's Open Source

$ git clone https://github.com/google/skywater-pdk

—> *Technology information availability is **virtually limitless***

—> *Leading to **massive open collaboration***

—> *Skywater 130nm PDK*

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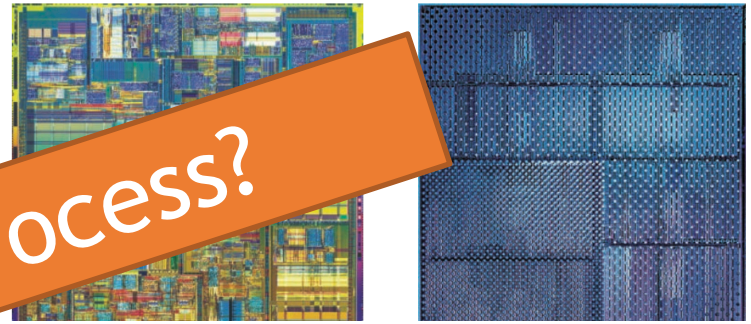
Intel Chips



What do I do with a 130nm process?

13

2000

Initial clock speed:
1.5GHz

Transistors:
42 million

Manufacturing technology:
0.18 micron

2001
Intel® Xeon® processor

Initial clock speed:
1.7GHz

Transistors:
42 million

Manufacturing technology:
0.18 micron

15

2003
Intel® Pentium® M processor

Initial clock speed:
1.7GHz

Transistors:
55 million

Manufacturing technology:
90nm

16

2006
Intel® Core™2 Duo processor

Initial clock speed::
2.66GHz

Transistors:
291 million

Manufacturing technology:
65nm

410 million

Manufacturing technology:
45nm

47 million

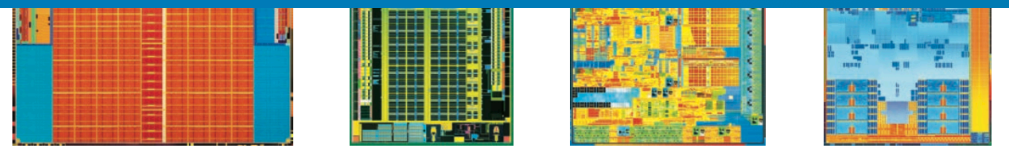
Manufacturing technology:
45nm

1.16 billion

Manufacturing technology:
32nm

1.4 billion

Manufacturing technology:
22nm



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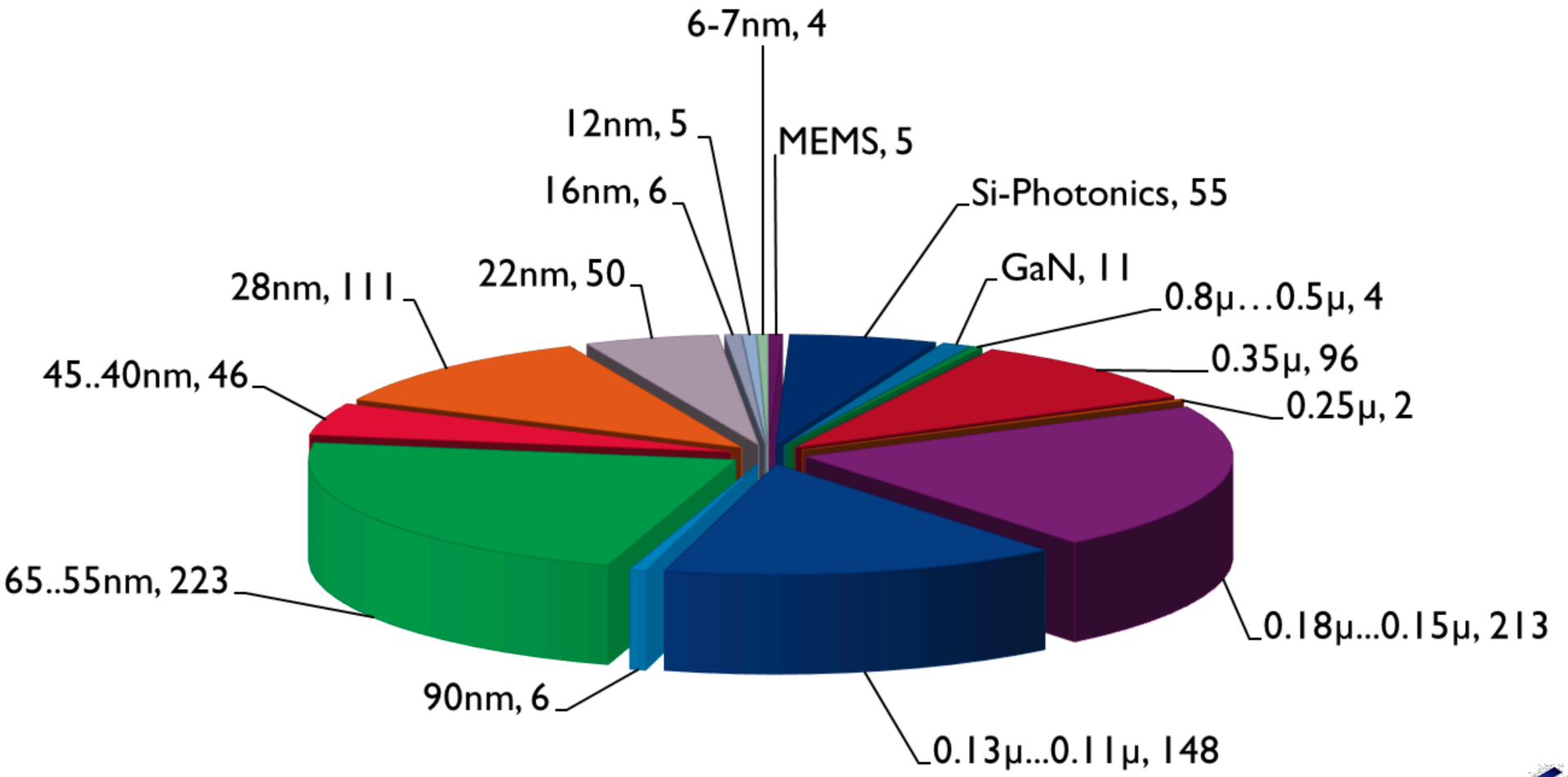
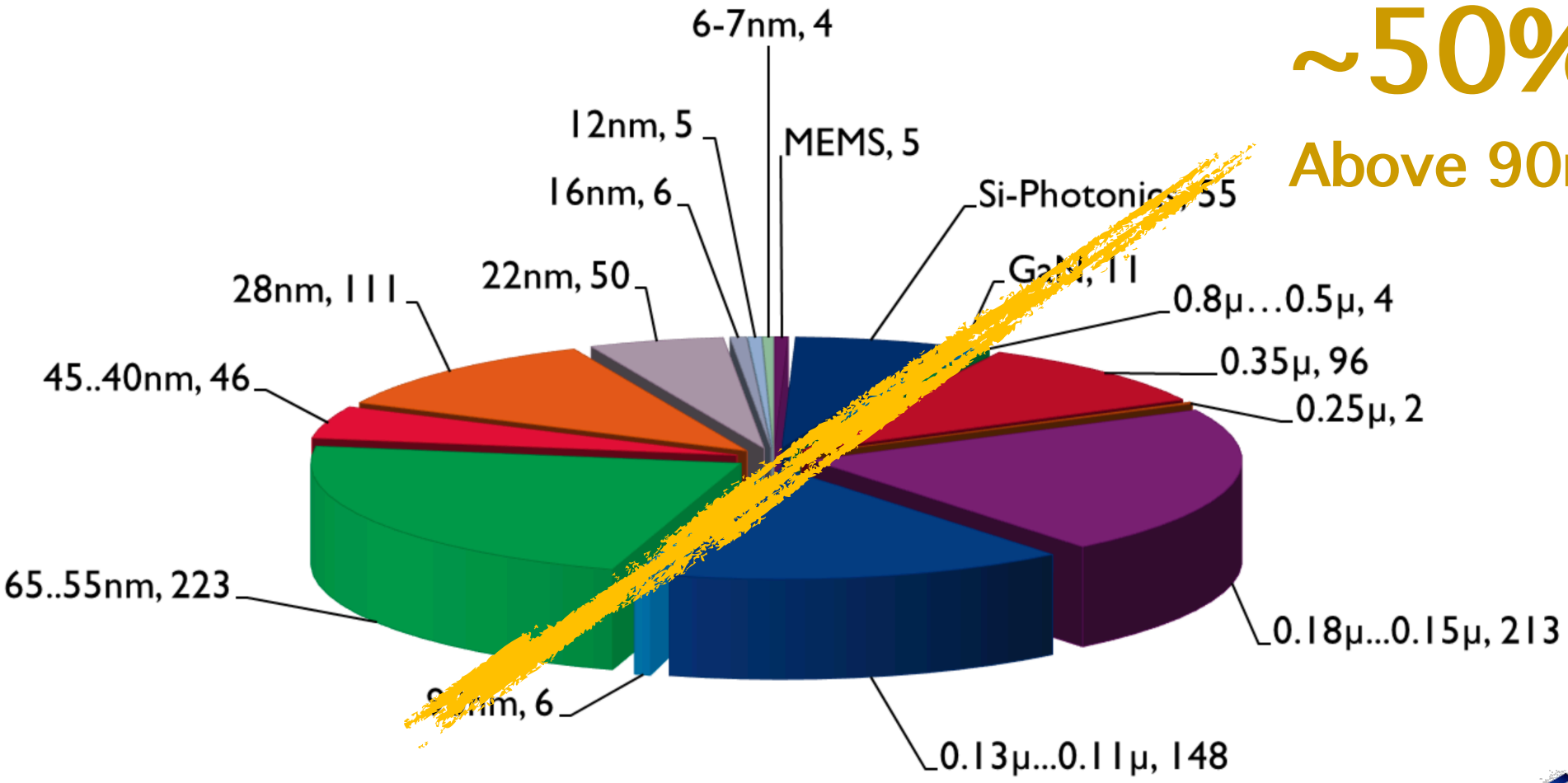
FABRICATION SERVICE (CIRCUITS 2021)



EUROPRACTICE has received funding from the European Unions H2020 Framework Programme for research, technological development and demonstration under grant agreement No 825121

FABRICATION SERVICE (CIRCUITS 2021)



~50%

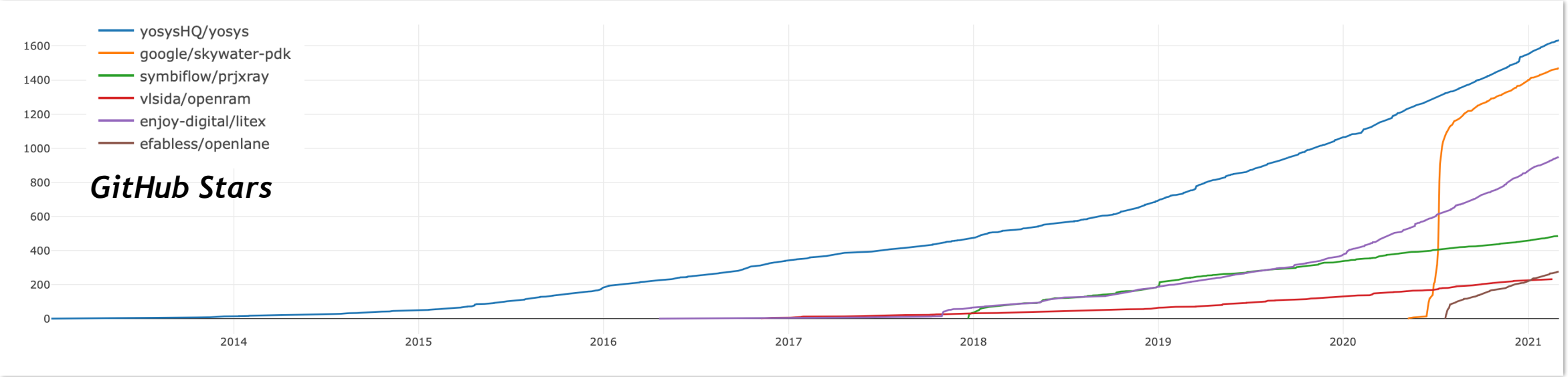
Above 90nm

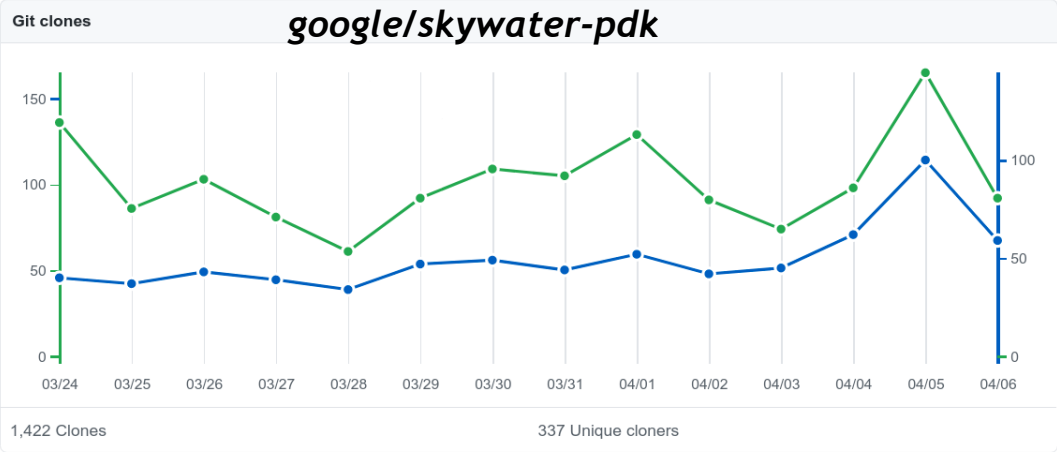
EUROPRACTICE has received funding from the European Unions H2020 Framework Programme for research, technological development and demonstration under grant agreement No 825121

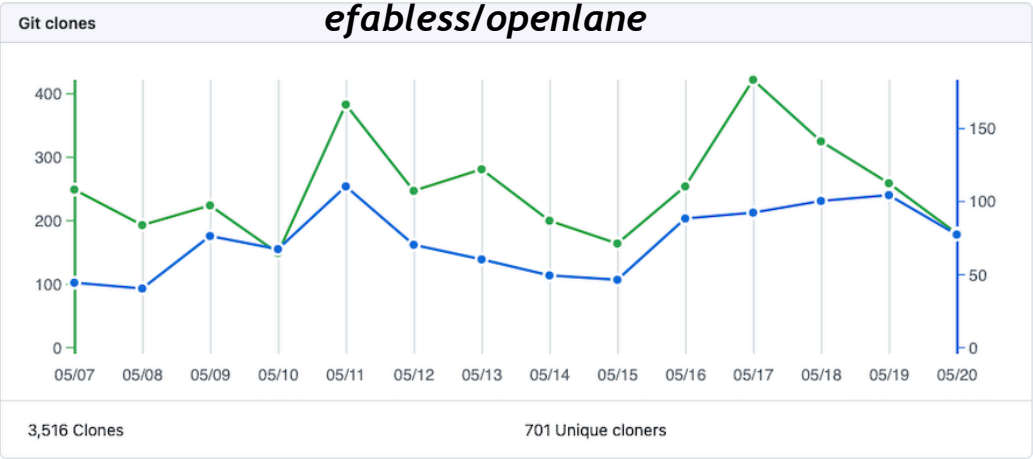
A LOT.....

See efabless.com/projects

SKY130 OPEN SOUCRE PDK WENT VIRAL







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LIVE SLACK COMMUNITY

3K+

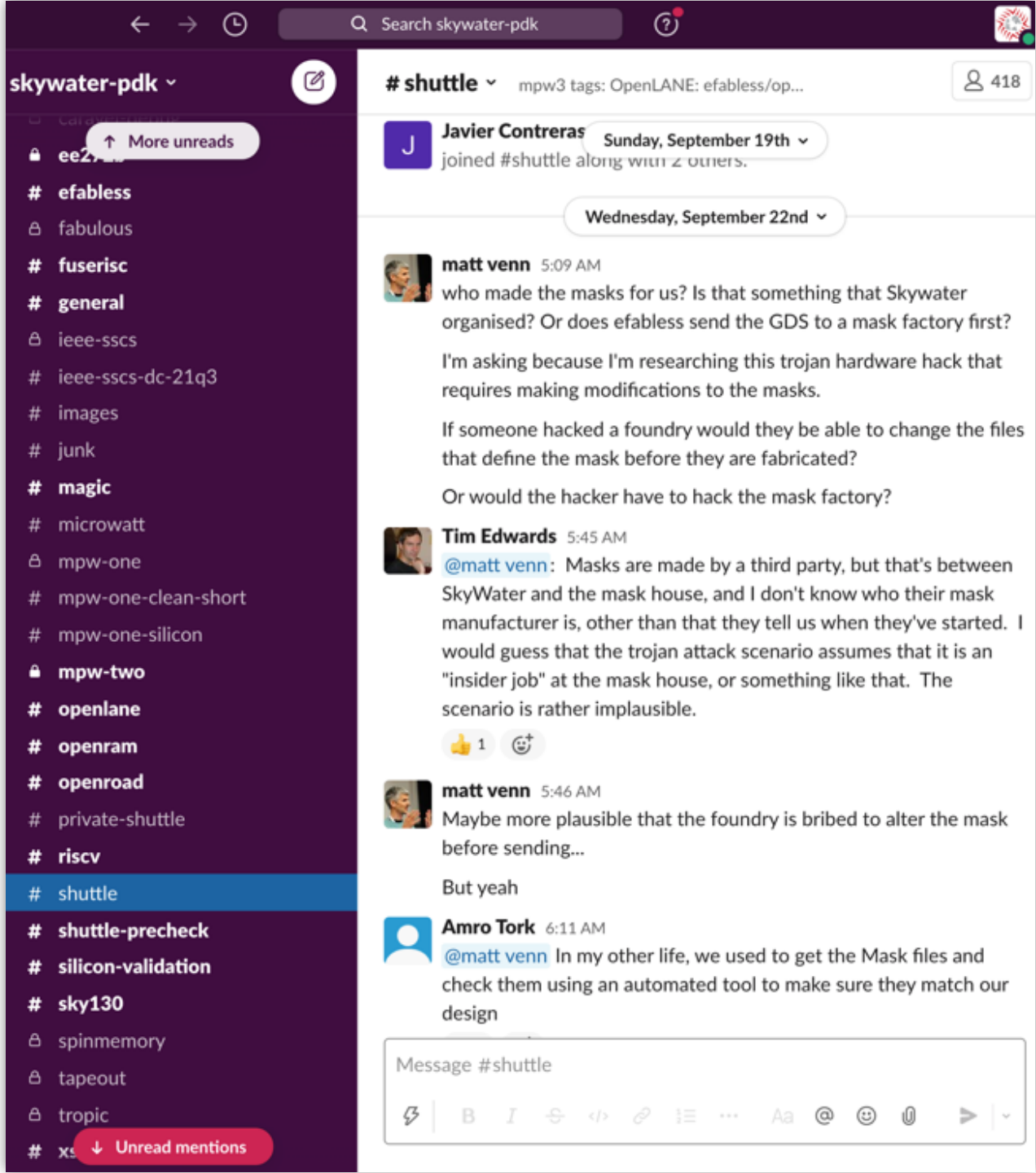
COMMUNITY MEMBERS

100+

CHANNELS & TOPICS

Join SkyWater-PDK Community

https://join.skywater.tools



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How do we simplify chip design? **#2**

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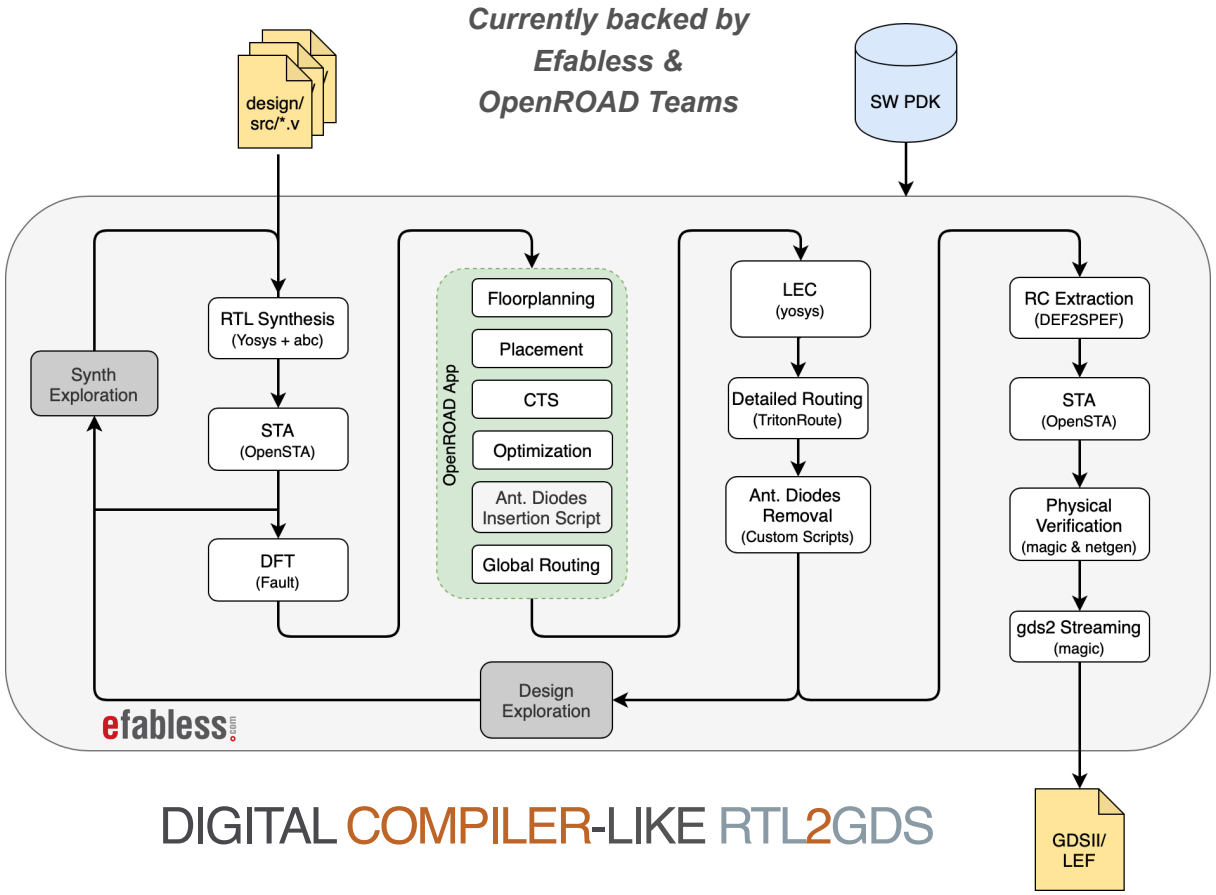
Codify and abstract knowledge

Automate code-to-chip like a ***GNU software compiler*** - *with trade-offs in area and performance.*

It opens the door for software developers to generate hardware

That's at least a 1000X more potential designers!



DIGITAL COMPILER-LIKE RTL2GDS

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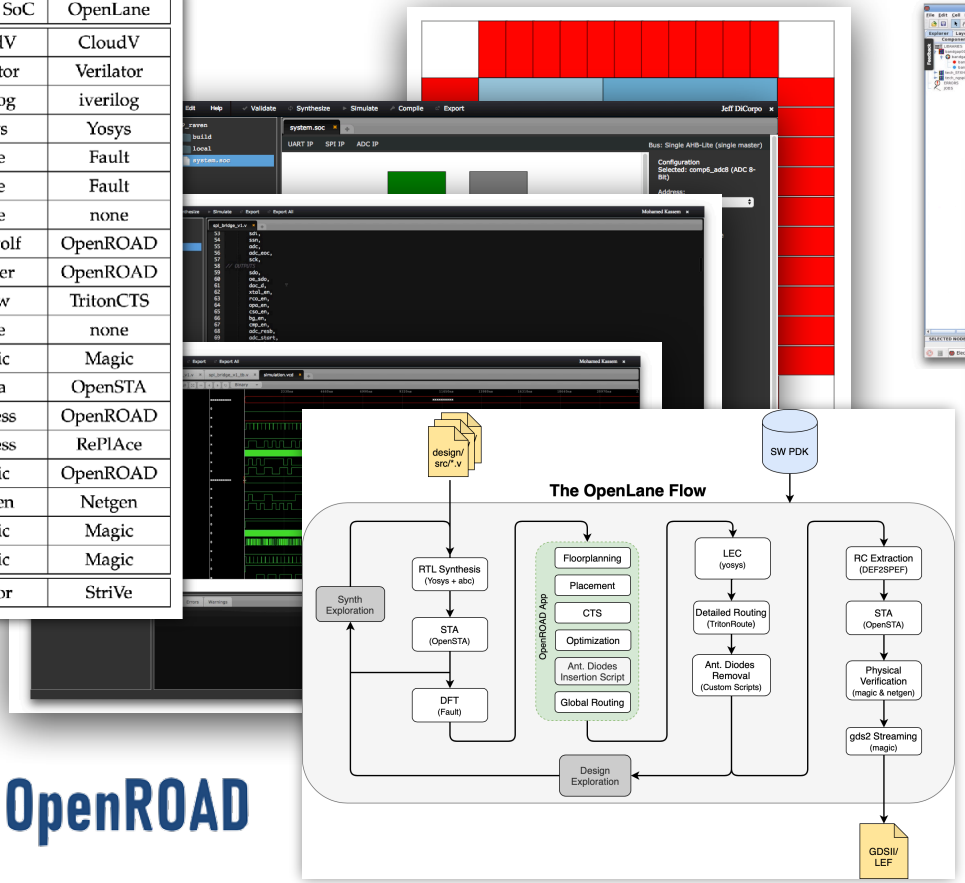
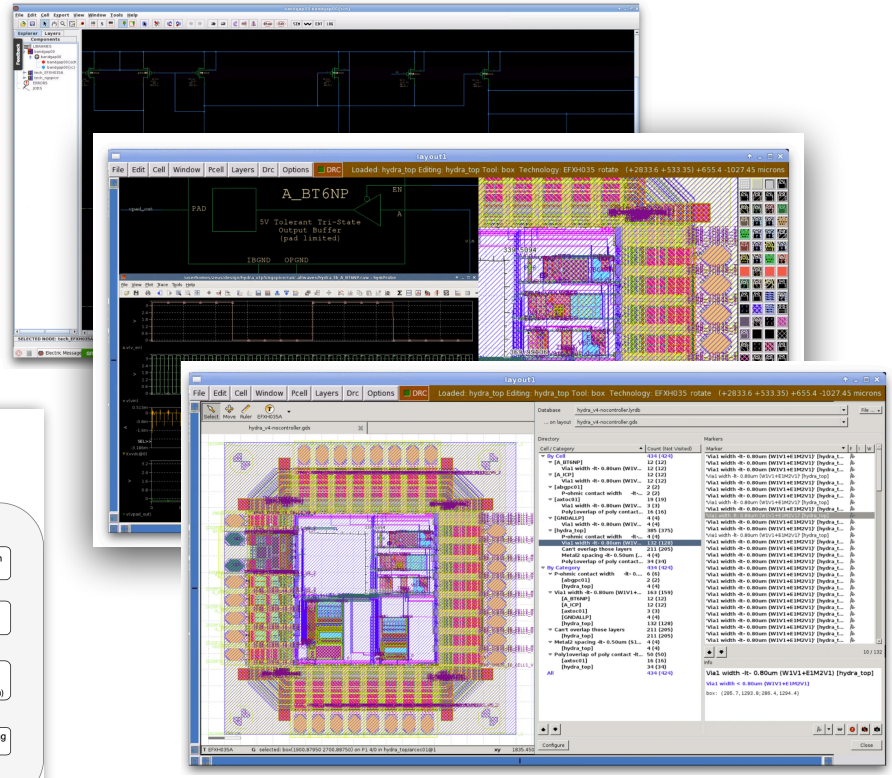
OPEN SOURCE DESIGN FLOWS & TOOLS

DESIGN STEP	Qflow	CloudV SoC	OpenLane
System Design	N/A	CloudV	CloudV
RTL Lint	Verilator	Verilator	Verilator
RTL Simulation	iverilog	iverilog	iverilog
Logic Synthesis	Yosys	Yosys	Yosys
DFT Scan Insertion	none	none	Fault
DFT ATPG	none	none	Fault
Formal Verification	none	none	none
Placement	graywolf	graywolf	OpenROAD
Routing	qrouter	qrouter	OpenROAD
CTS	Qflow	Qflow	TritonCTS
Dynamic EMIR	none	none	none
Extraction	Magic	Magic	Magic
Timing Analysis	Vesta	Vesta	OpenSTA
Floorplanning	Magic	efabless	OpenROAD
Top-Level Placement	Magic	efabless	RePlAce
Top-Level Routing	Magic	Magic	OpenROAD
LVS	Netgen	Netgen	Netgen
DRC	Magic	Magic	Magic
GDS	Magic	Magic	Magic
SoC	Raven	Raptor	StriVe





- SoC Editor
- RTL Simulation
- Synthesis
- GL Simulation

OpenROAD

- Schematic Capture
- SPICE Simulation

- Mixed-Mode Simulation
- Parasitic Extraction
- Physical Verification

Silicon Compiler Coriolis OpenLane

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ANALOG TRANSISTOR-LEVEL

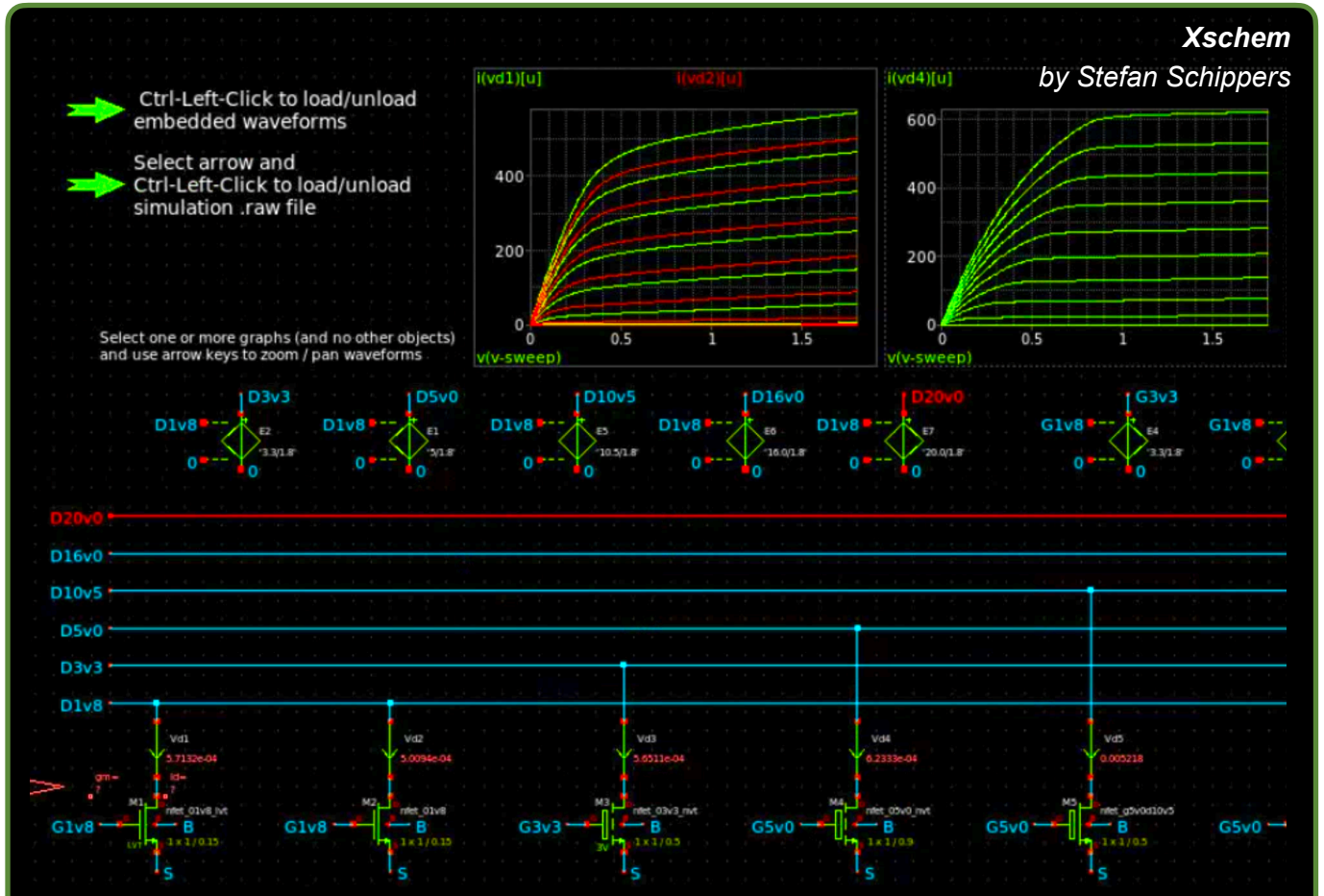
Analog transistor-level design, schematic and layout

Schematics: Xschem

Simulators: ngspice, Xyce

Support: Process Corners and statistical simulations

Packed with out-of-the-box examples - just click, copy and run yours



*SPICE Simulations with **ngspice** or **Xyce** for **SKY130***

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Why does it matter to have tools open-sourced?

***Limitless availability** which fosters **spontaneous idea realization** and open **collaborative** development by community*

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How do we simplify chip design? **#3**

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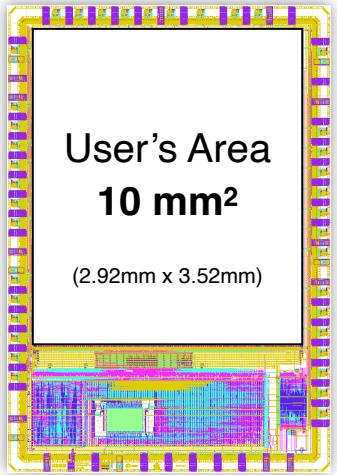
Start from the 15th floor to reach 20

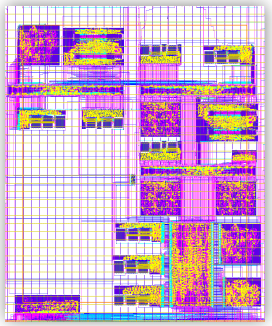
*Build on existing foundational work by others - **CARAVEL***

*You only need to know your design … or **your code***

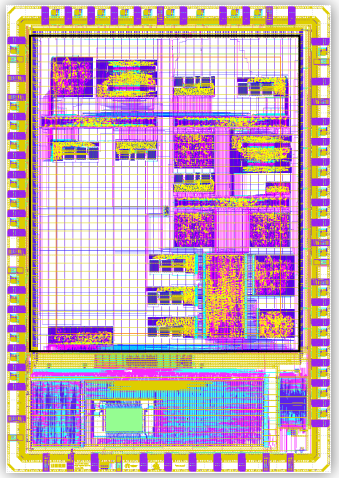


CARAVEL

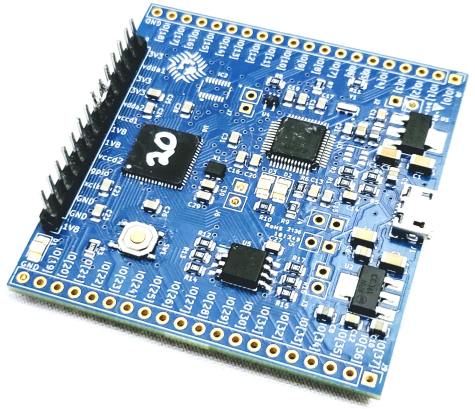
+



My Design



CARAVEL + My Design



Plug & Play Dev Board

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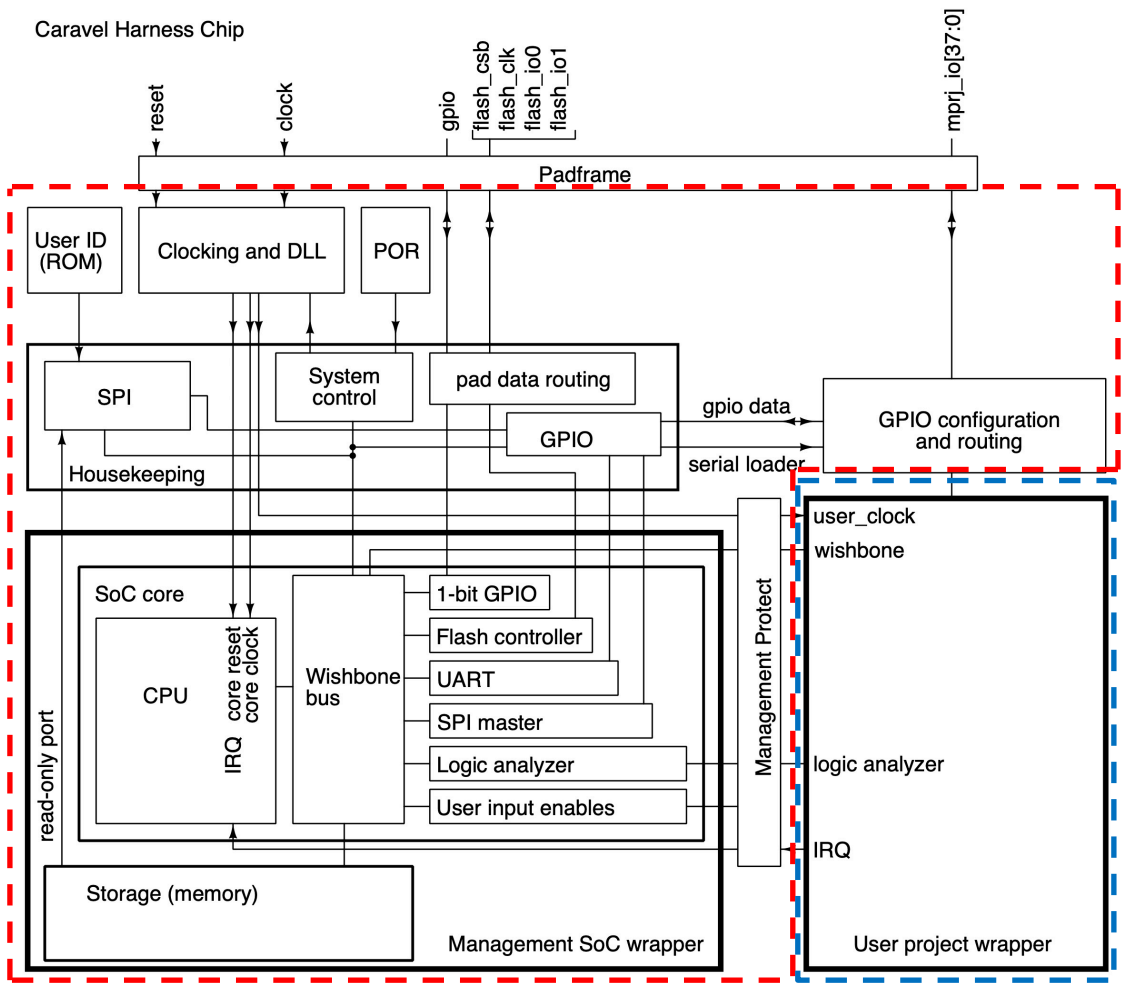
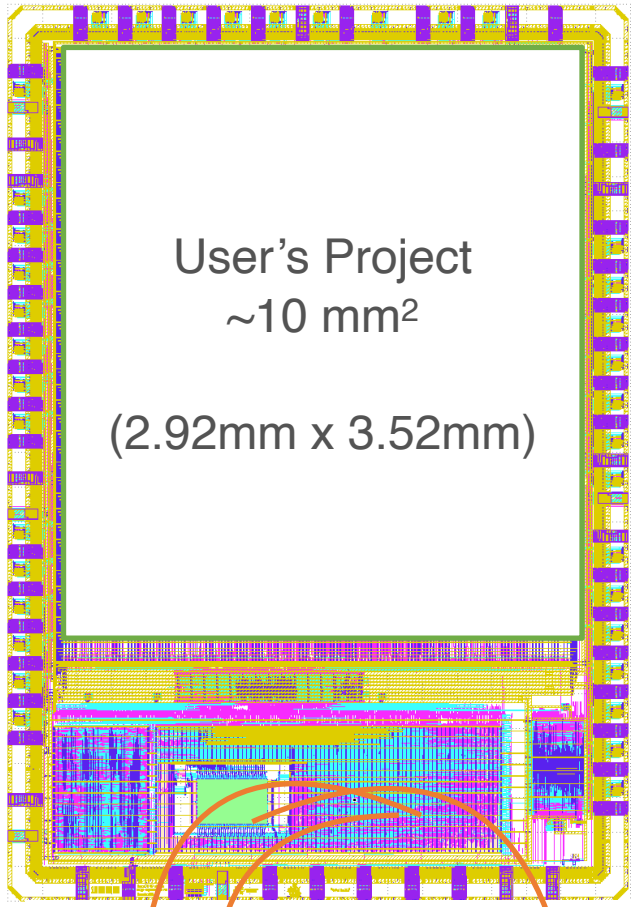
CARAVEL PLATFORM



https://github.com/efabless/caravel

CARAVEL SoC Platform



PicoRV32 OpenRAM
OpenROAD OpenLane

Uniform Open Source File Structure to ease reuse & modifications

- .github/workflows
- .travisCI
- def
- docs
- gds
- irsim
- lef
- lvs
- macros
- mag
- maglef
- ngspice
- oas
- openlane
- qflow
- scripts
- signoff
- spef
- spi/lvs
- utils
- verilog
- xyce

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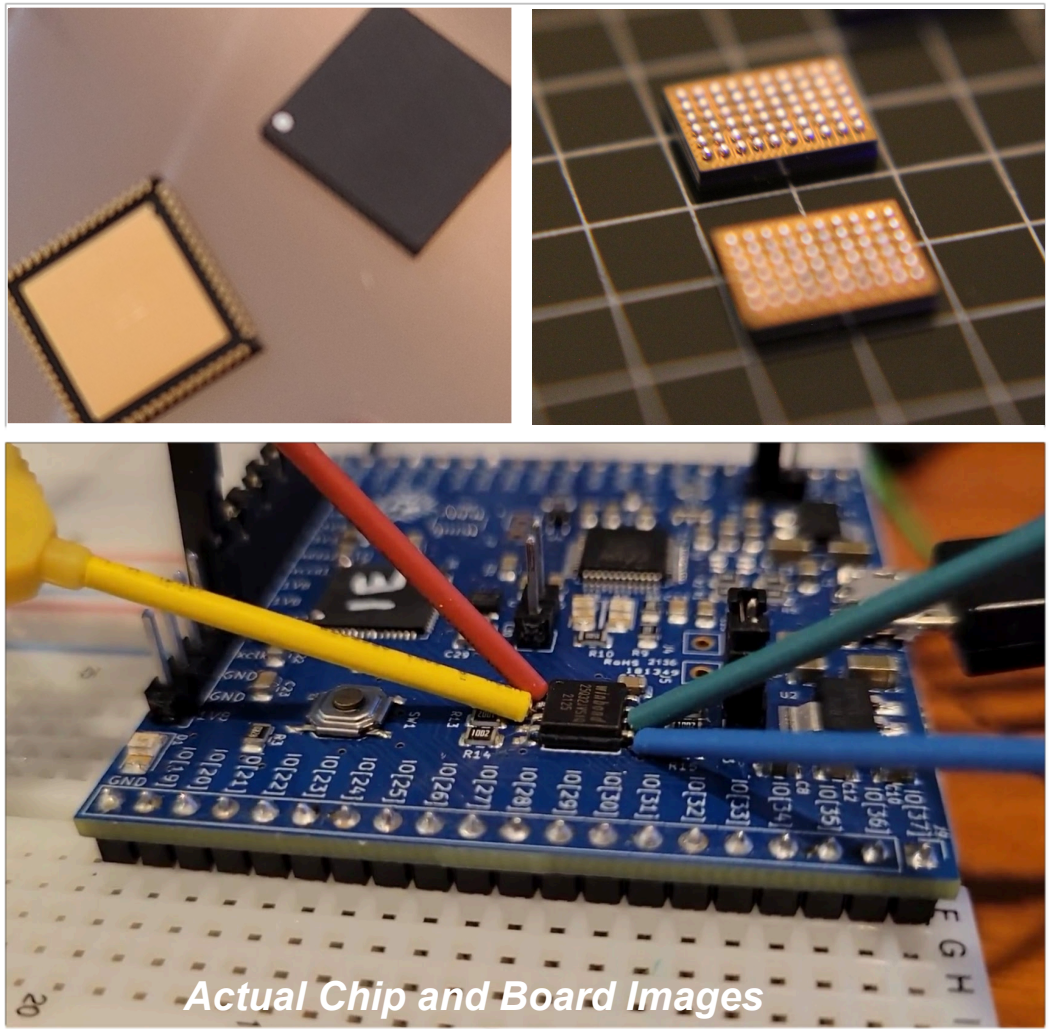
SILICON TESTING & VALIDATION



Actual Chip and Board Images

Designers receive **packaged chips** and **assembled 5 evaluation boards** with for each project

On-chip **open source** test framework with firmware to support the following:

- On-chip logic Analyzer
- Drivers for common peripherals
- Flash memory programming software utility
- Example firmware routines for common functions
- Instructions for customizing firmware for each project

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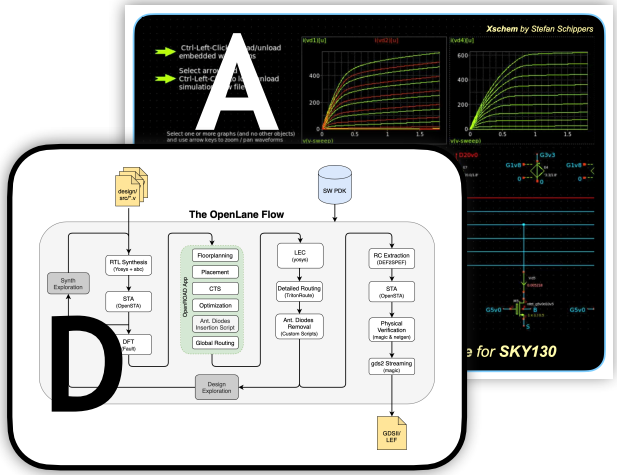
OS EDA Digital & Analog

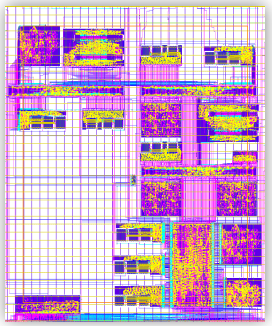


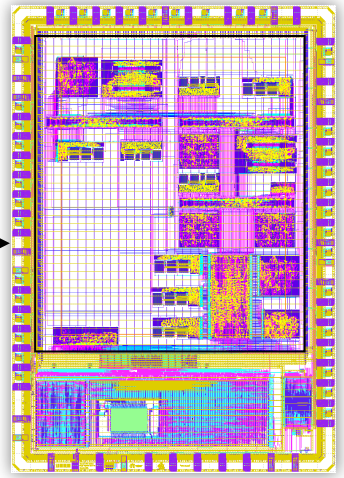
+

CARAVEL

+

User Design





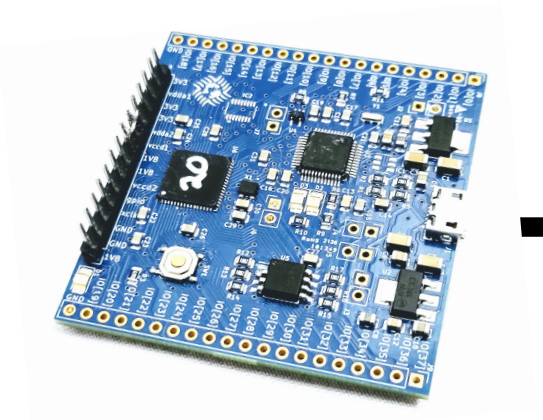
CARAVEL + User Design

MANUFACTURING

Start Here
https://ef.link/start-digital
https://ef.link/start-analog

Software (FOSS)

+



5 Dev Boards

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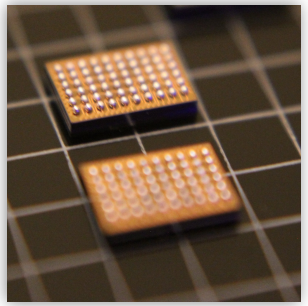

300 WCSP Parts

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How do we simplify chip design? **#4**

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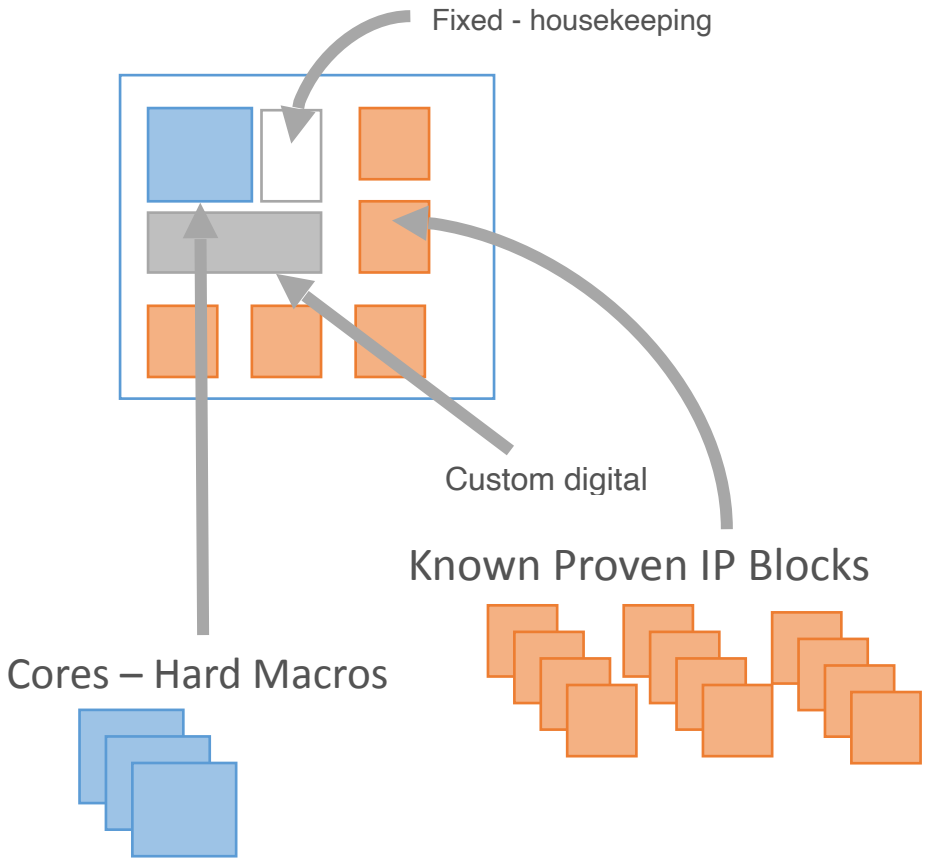
Build an open library of “IP blocks”

Make them like LEGO

- Silicon proven / verified functions
- Highly leveraged known proven IP blocks
- Scope of customization is constrained
- Quality processes enable extending the known proven IP blocks by community



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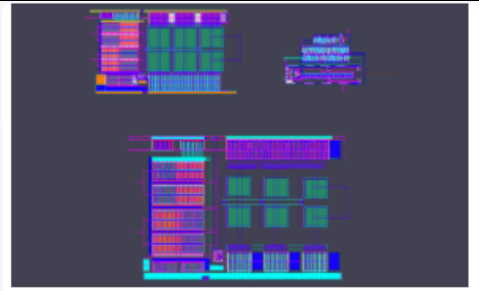
Select Open Source Designs

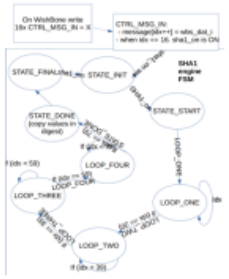


caravel_fulgor_opamp public

Diego Hernando | http://www.fundacionfulgor.org.ar/sitio/index.php

Operational amplifier (opamp) based on the Miller topology designed in Skywater SKY130 CMOS process.

MPW-1 SKY130 2.2k

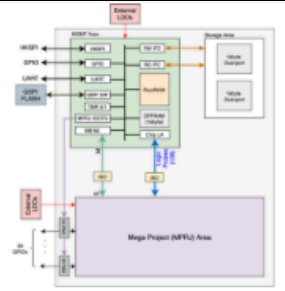


SHA1 engine public

Konrad Rzeszutek Wilk

The SHA1 engine, while not the most secure nowadays is still used by git commits and TPM PCR...

MPW-2 SKY130A 731

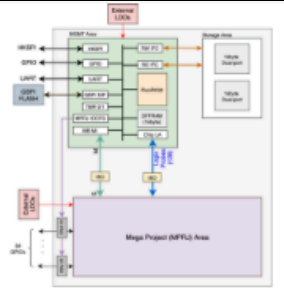


Caravel-SOFA-HD public

Xifan Tang | https://sites.google.com/site/pegaillardon/home

SOFA-HD (Skywater Opensource FPGAs)

MPW-1 SKY130 1.6k

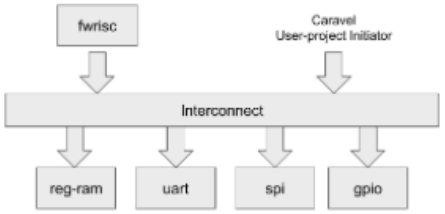


Caravel public

Sylvain Munaut | https://github.com/PyFive-RISC-V

Peripherals tests for future SoC targeting Micro/Circuit Python

MPW-1 SKY130 1.8k

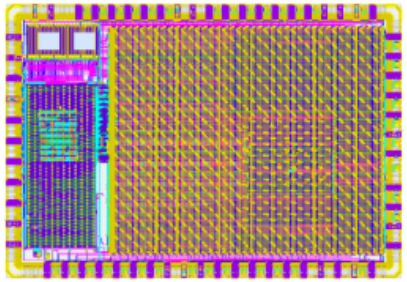


FWPayload public

Matthew Ballance | http://github.com/mballance

A simple RISC-V core+peripherals subsystem for the Google-sponsored Open MPW shuttles for SKY130.

MPW-1 SKY130 962

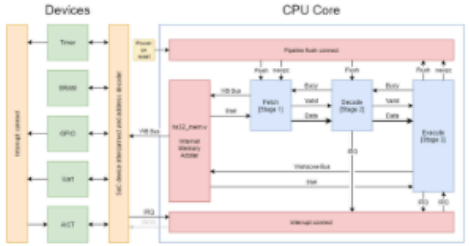


Caravel_Astria_Testchip public

Astria Nur Irfansyah | http://www.its.ac.id

Test circuits consisting of synthesizable comparators for a stochastic ADC, to be submitted for...

MPW-1 SKY130 1.2k

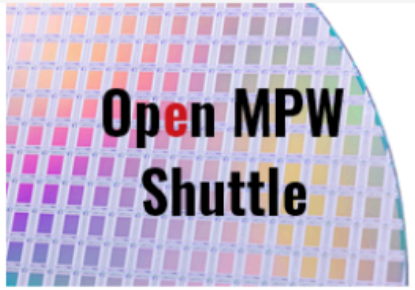


HS32Core public

Kevin Mack Baragona | https://github.com/hsc-latte

Open Source Hardware Processor

MPW-1 SKY130 1.4k

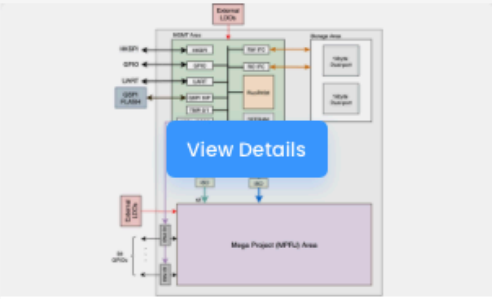


10_bit_potentiometric_DAC public

Sameer S Durgoji | https://www.vlsisystemdesign.com/

Design of a 10 Bit Potentiometric Digital to Analog Converter with 3.3V analog voltage, 1.8V...

MPW-2 SKY130A 1.1k

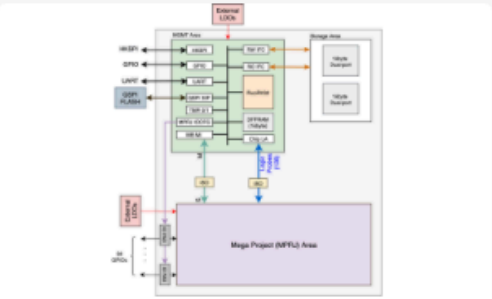


Caravel-SOFA-CHD public

Xifan Tang | https://sites.google.com/site/pegaillardon/home

SOFA-CHD (Skywater Opensource FPGAs)

MPW-1 SKY130 917

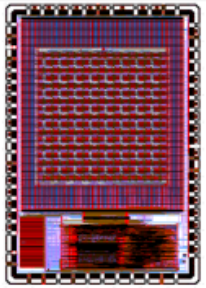


Caravel_RISCV_OSU public

James Stine | https://vlsiarch.ecen.okstate.edu/

Caravel_RISCV_OSU is an implementation of a single-cycle RISC-V processor inside of the Caravel...

MPW-1 SKY130 1.2k

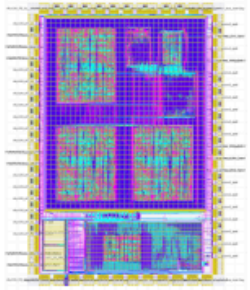


Caravel-OpenFPGA-EF public

Manar Abdelatty | http://efabless.com

A template SoC for Google sponsored Open MPW shuttles for SKY130.

MPW-1 SKY130A 1.8k

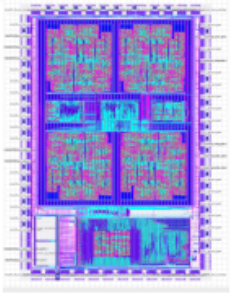


Chameleon SoC public

M. Shalan | http://efabless.com

AHB-Lite based SoC for IBEX

MPW-1 1.2k

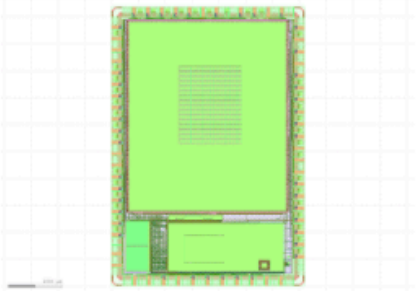


Caravel public

M. Shalan | http://efabless.com

NFive32-Based SoC to validate several open-source projects and IPs.

MPW-1 1.4k

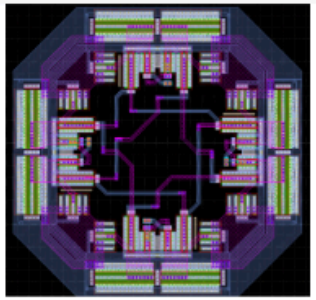


MorphleLogic public

Merik Voswinkel | http://www.fiberhood.org

A test-wafer for testing Mophle Logic reconfigurable hardware for SKY130.

MPW-1 SKY130 1.4k

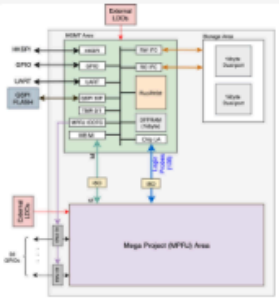


caravel_amsat_txrx_ic public

Thomas Parry | N/A

Amatuer Radio Satellite Transceiver (SKY130) - Caravel Submission

MPW-1 SKY130 2.8k



Softshell public

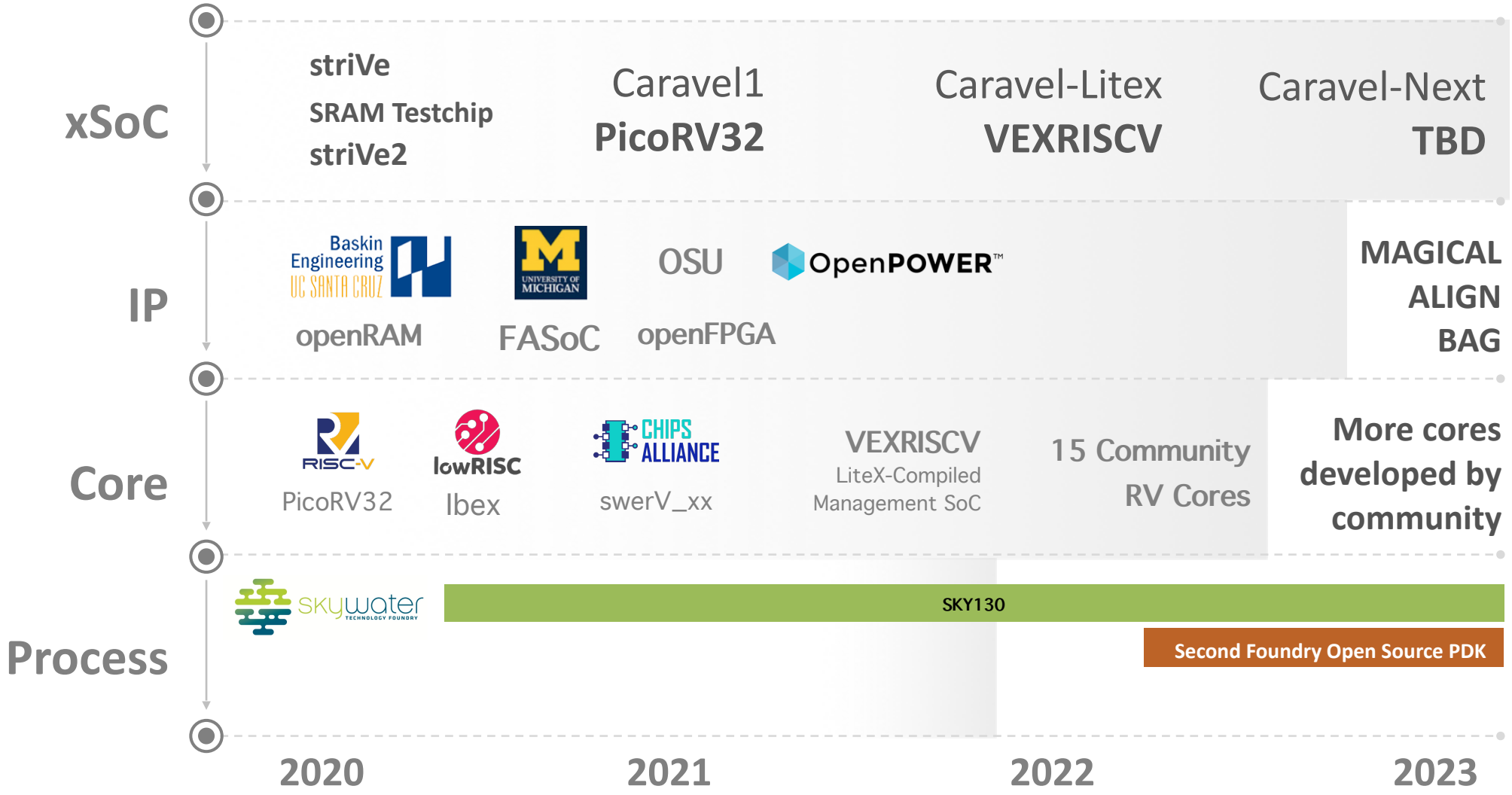
Harrison Pham | https://harrisonpham.com/

Multicore MCU for implementing software defined peripherals.

MPW-1 SKY130 1.7k

Select Open Source Designs

OPEN SOURCE ECOSYSTEM AT WORK



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How do we simplify chip design? **#5**

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OK - sounds good so far

but … manufacturing cost $$

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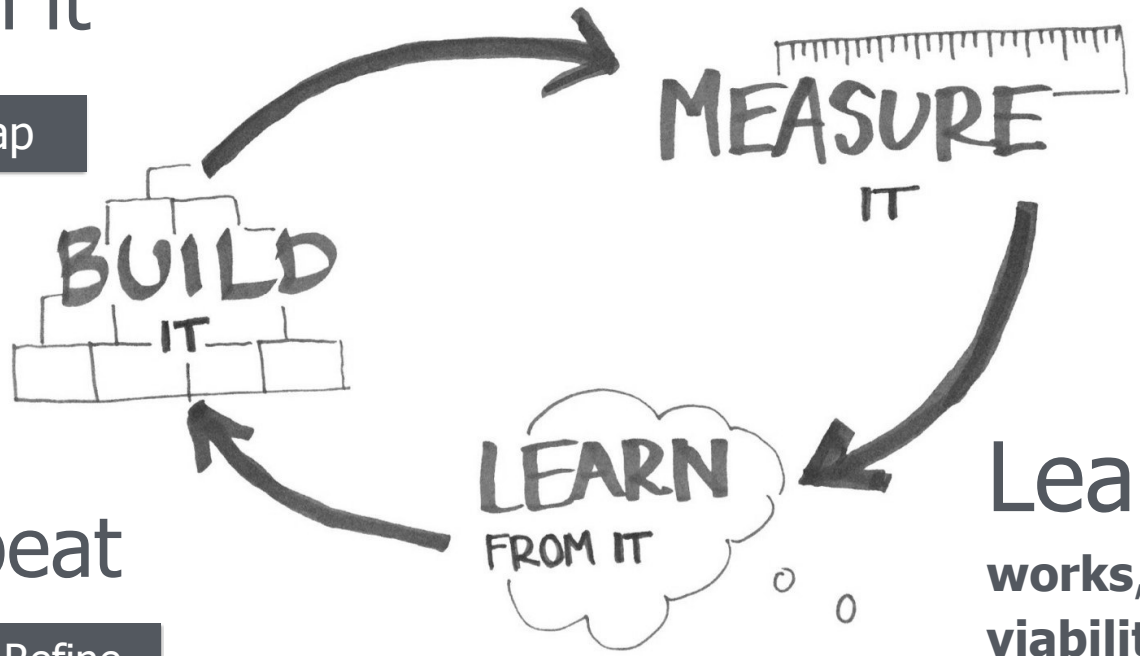
Enable —Fail fast, learn and repeat

1 Design it

Quick & Cheap



Test It **2**

Learn from it, What **works**, What **doesn't** **viability** and feasibility **3**

4 Repeat

Correct & Refine

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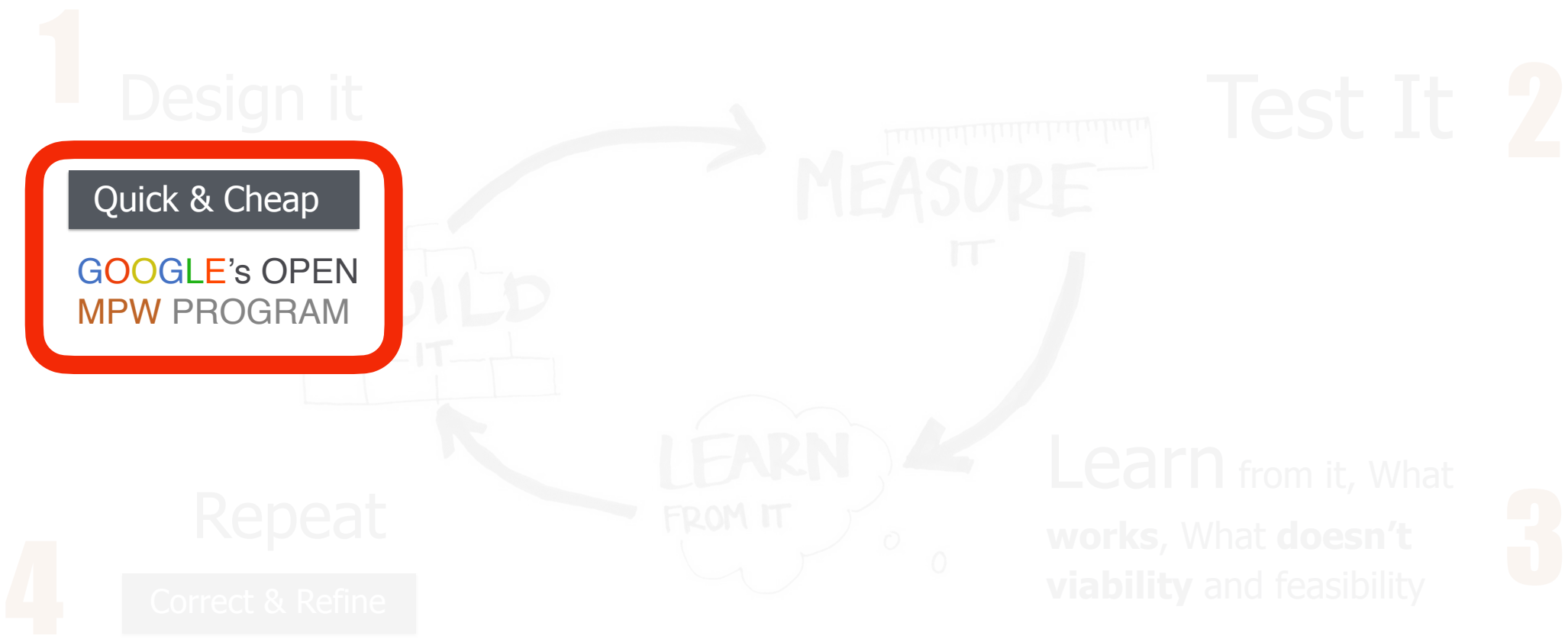
Enable —Fail fast, learn and repeat



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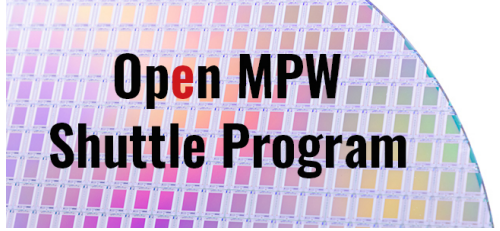
GOOGLE's OPEN MPW PROGRAM



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Sponsored by Google

- **Google** is funding **4** manufacturing runs in **2022** - minimum of **40** designs each
- Participants use an Harness SoC (Caravel) with ***10mm2 open area***
- SKY130 Open Source Digital & Analog Design Tools are available
- Participants get ***5 dev boards + 300 WCSP-packaged parts***
- All designs must be public and under an ***open source license***
- All designs must contain information & files to ***reproduce the work***
- Participants are strongly encouraged to try new ideas, ***take risks and iterate***
- All skill and experience levels are welcome to participate

Start here https://ef.link/gmpw

Join the community at https://ef.link/chat

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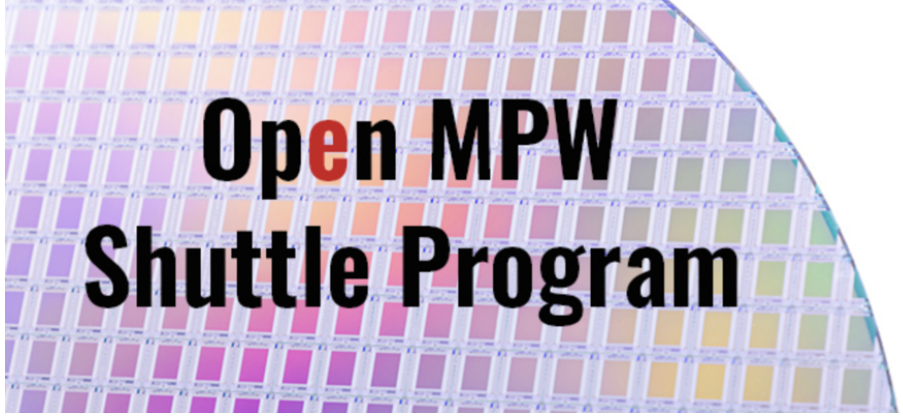
The first shuttle was overbooked: 45 designs submitted in 30 days!



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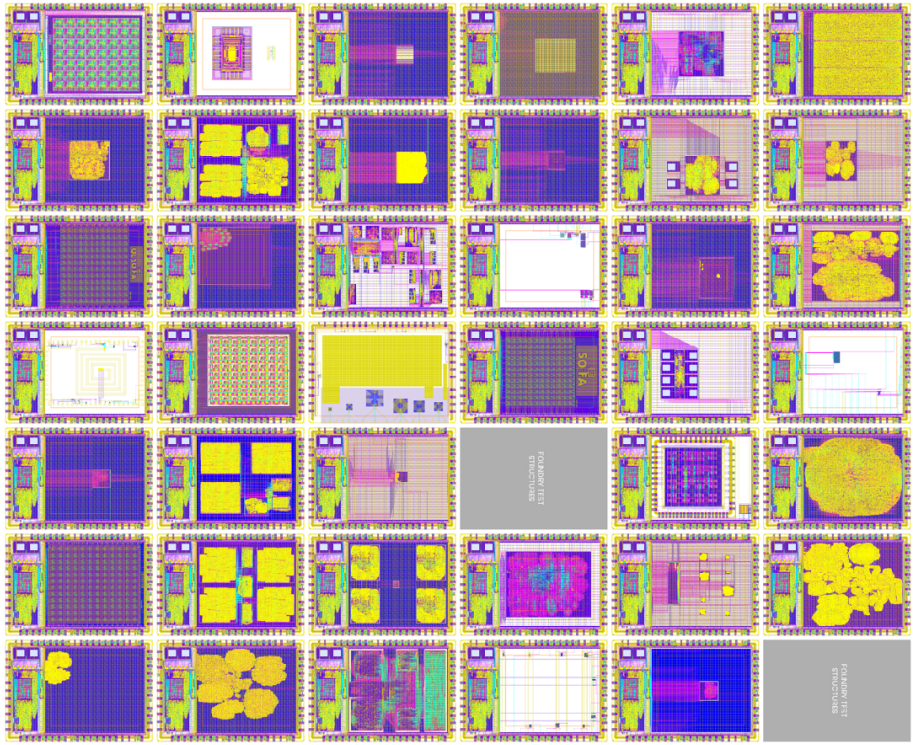

DESIGN TYPES

- 9 x Open processor cores
- 9 x SoC's
- Crypto-currency Miner
- Robotic App Processor
- Amateur Satellite Radio Transceiver
- 7 x Analog/RF
- 5 eFPGA's

MPW ONE

See Projects Here: https://efabless.com/projects/shuttle_name/MPW-1

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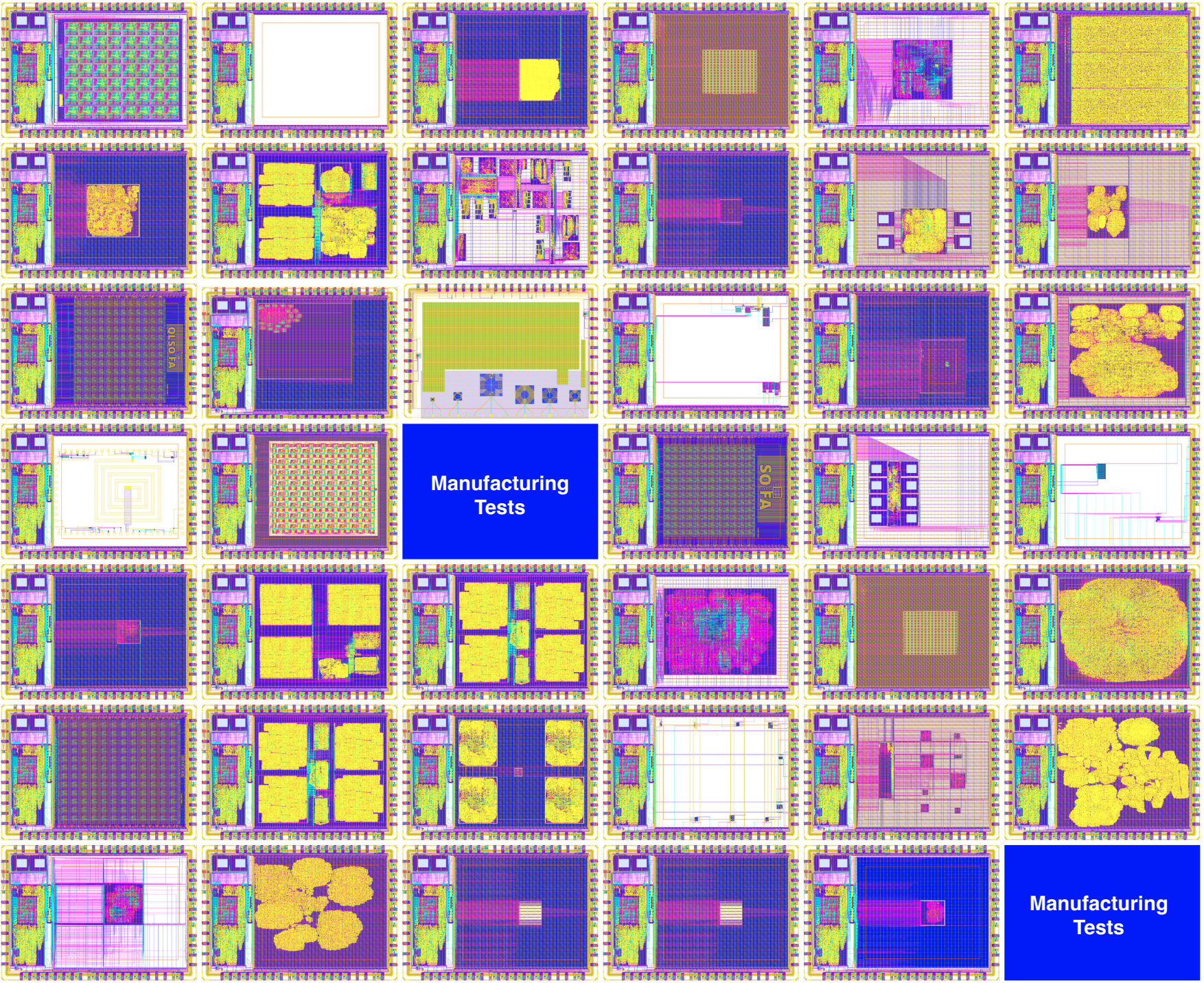


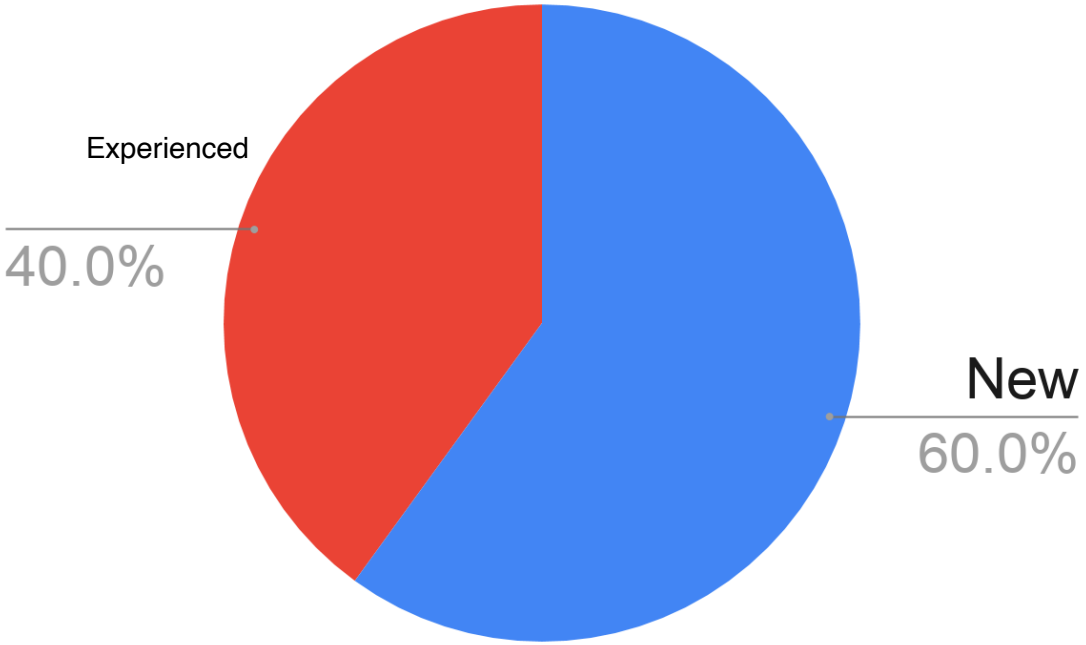
DESIGN TYPES

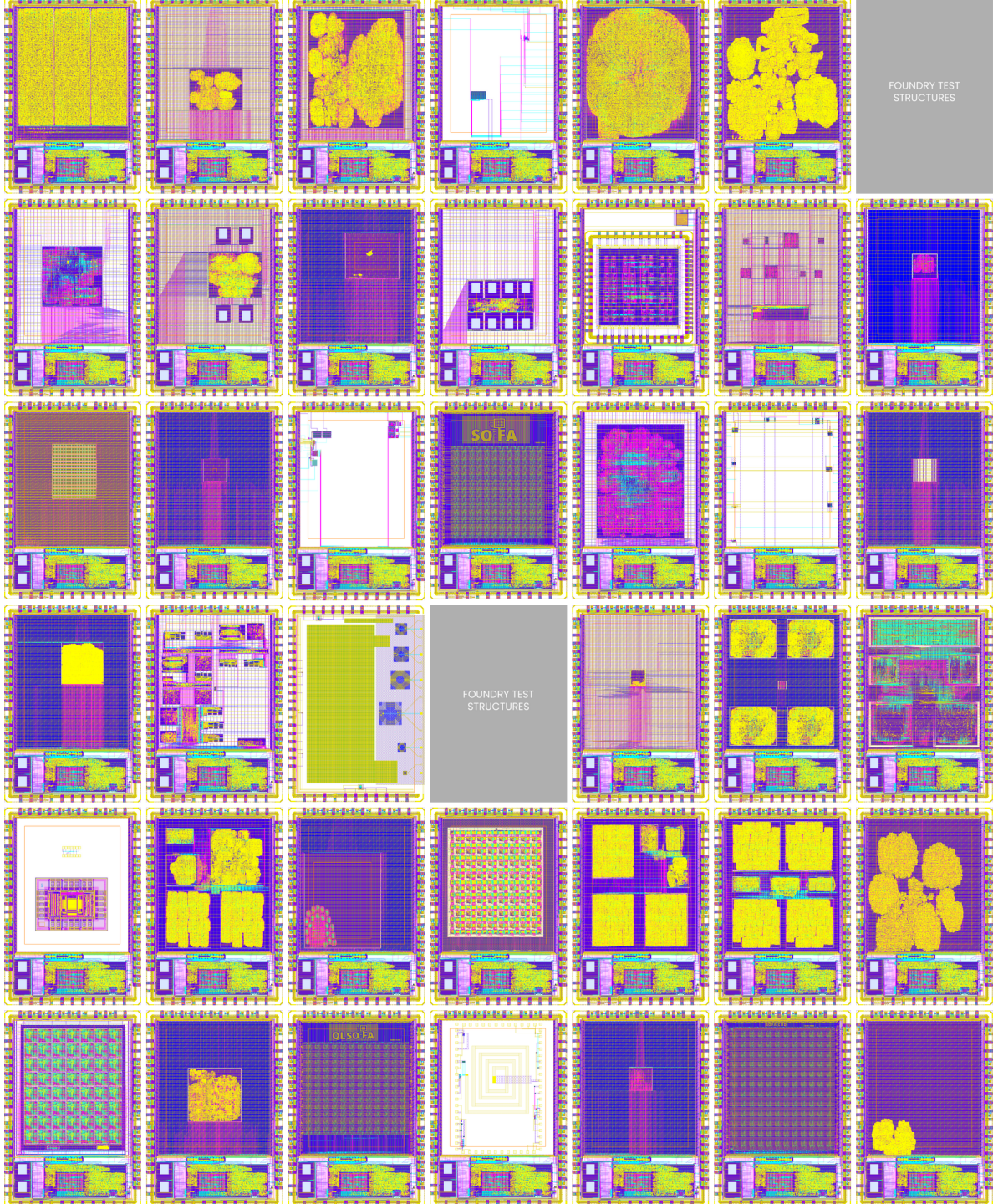
- 9 x Open processor cores
- 9 x SoC's
- Crypto-currency Miner
- Robotic App Processor
- Amateur Satellite Radio Transceiver
- 7 x Analog/RF
- 5 eFPGA's

COMPANIES

- IBM: OpenPOWER - MicroWatt
- QuickLogic - eFPGA
- Antmicro
- Western Digital - Swerv-EL2
- EFabless
- SpinMemory

60% by first time designers!



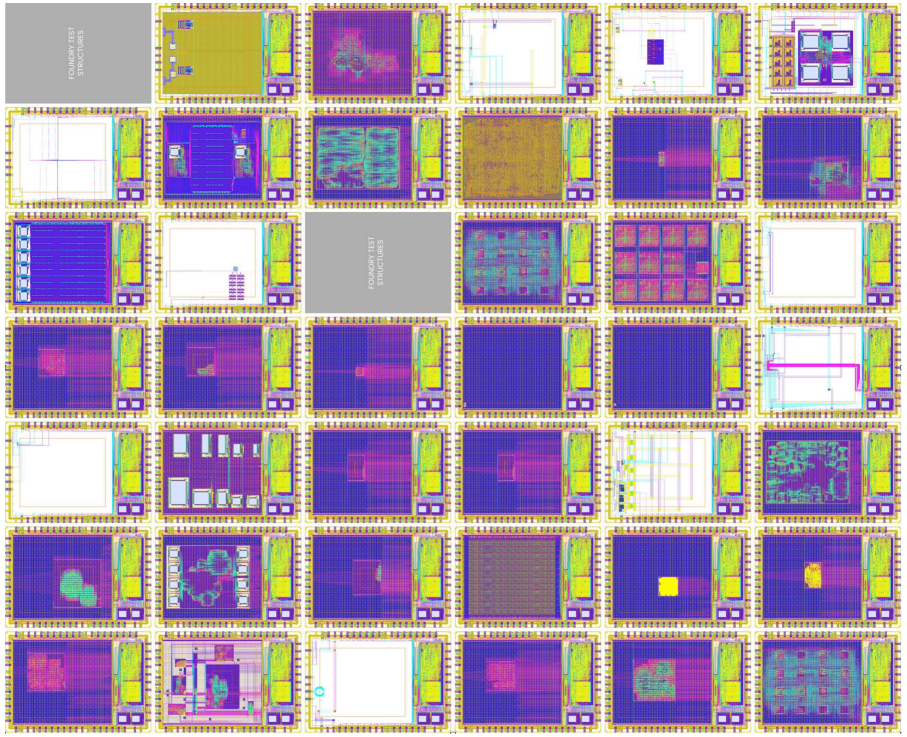


And so was the second:
56 designs submitted
in 30 days!

Open MPW Shuttle Program

efabless.com

Sponsored by Google



DESIGN TYPES

- 11 x Open processor cores
- 11 x SoC's
- Crypto-router
- T2D Converter - LIDAR
- Multi-project harness for Caravel x 16
- 17 x Analog/RF
- 2 eFPGA's

MPW TWO

See Projects Here: https://efabless.com/projects/shuttle_name/MPW-2

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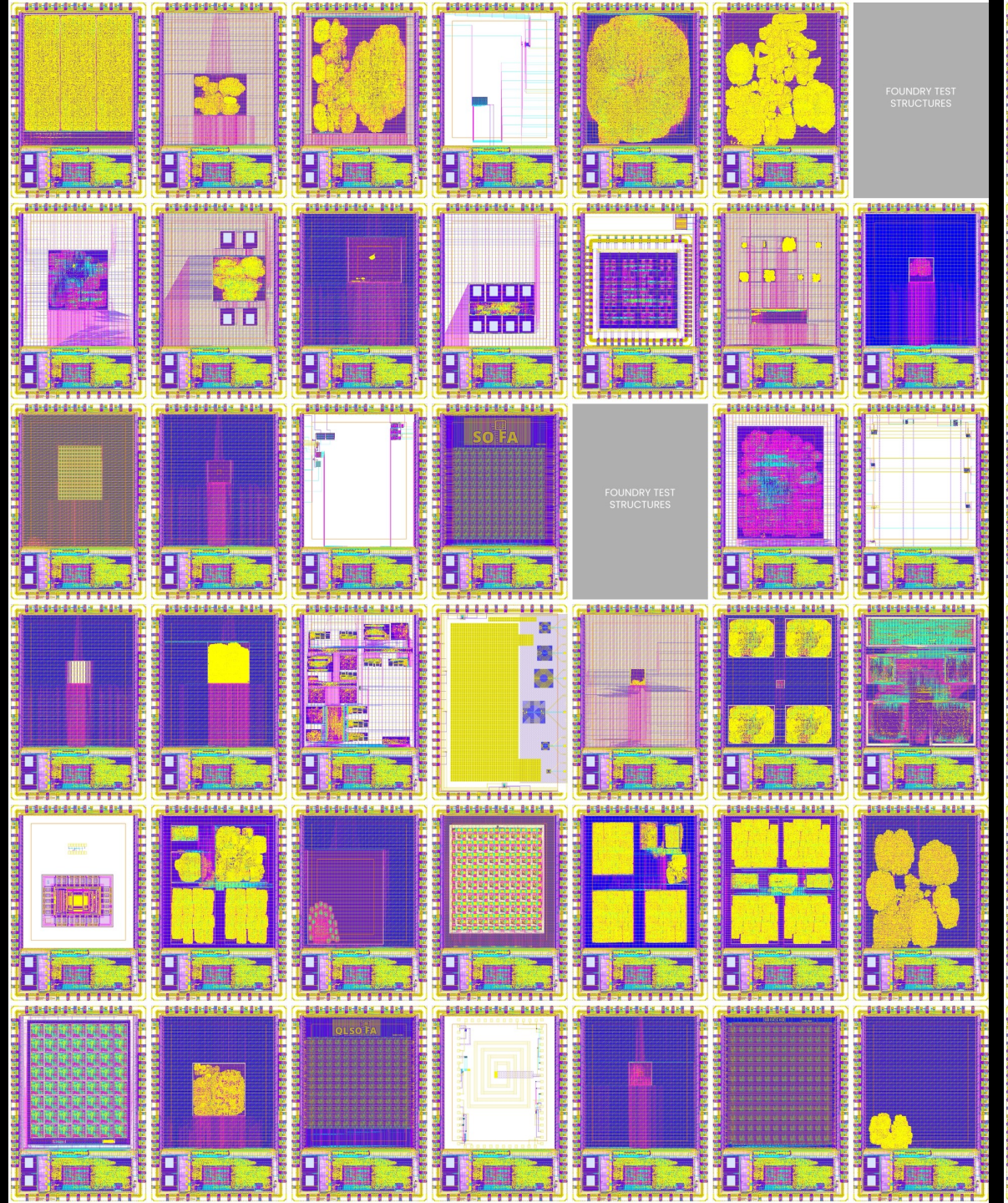
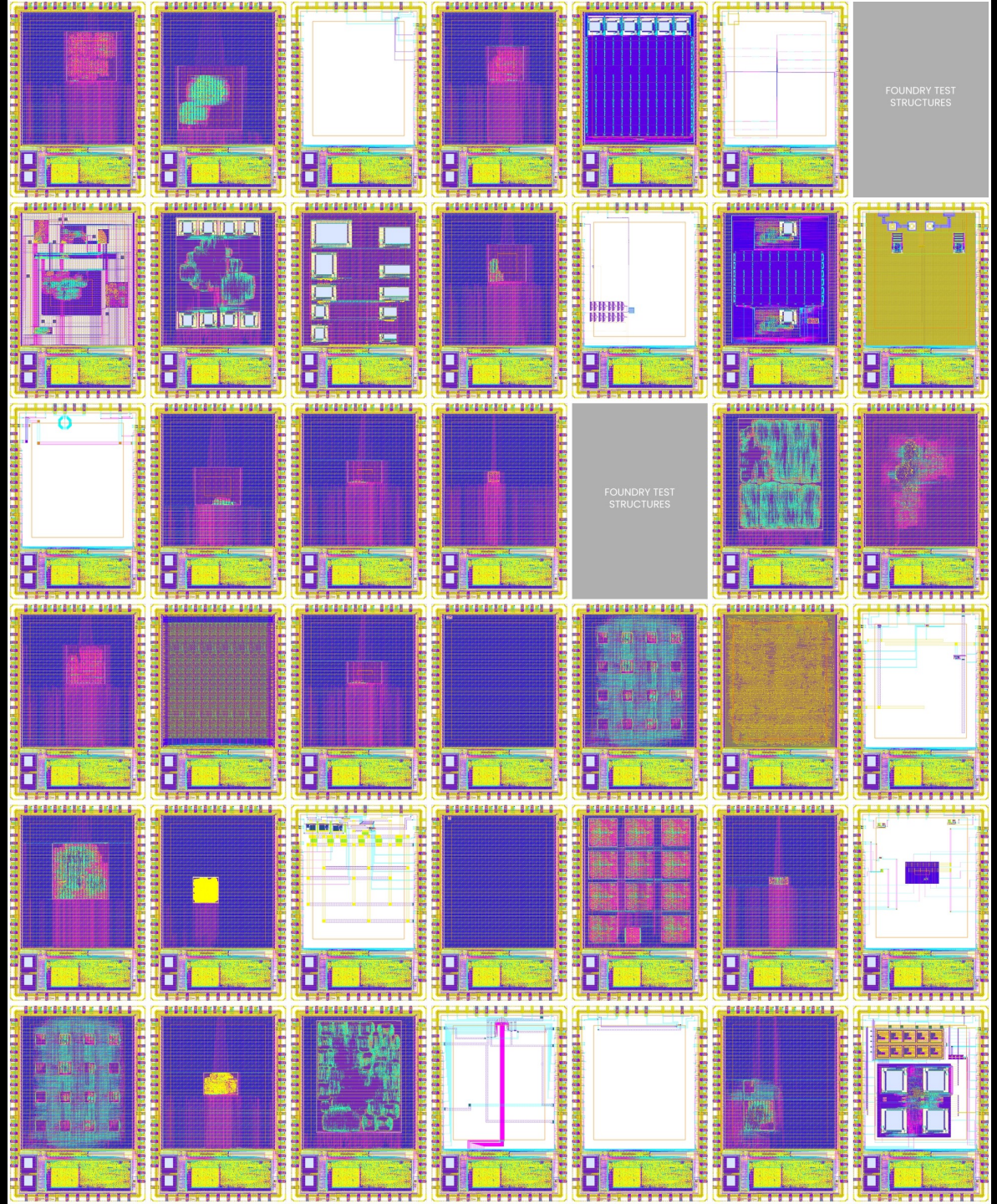
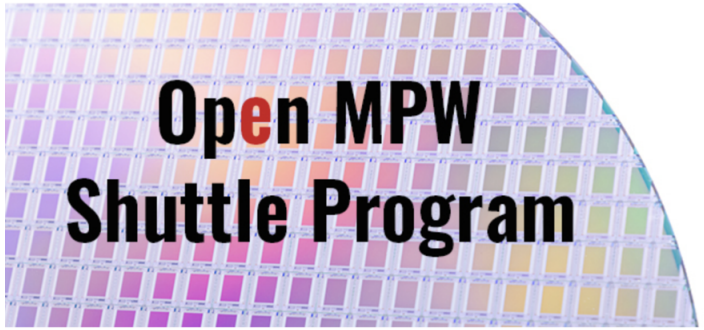
MPW ONE





MPW TWO



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WELCOME TO THE EFABLESS OPEN MPW SHUTTLE PROGRAM

Universities Put Fabrication into Courses and Drive Research and Early Innovation

Companies Advance and Showcase their Innovations

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OpenMPW Project Submissions

Always Overbooked

45	56	52	55	77
MPW-1	MPW-2	MPW-3	MPW-4	MPW-5

https://efabless.com/projects

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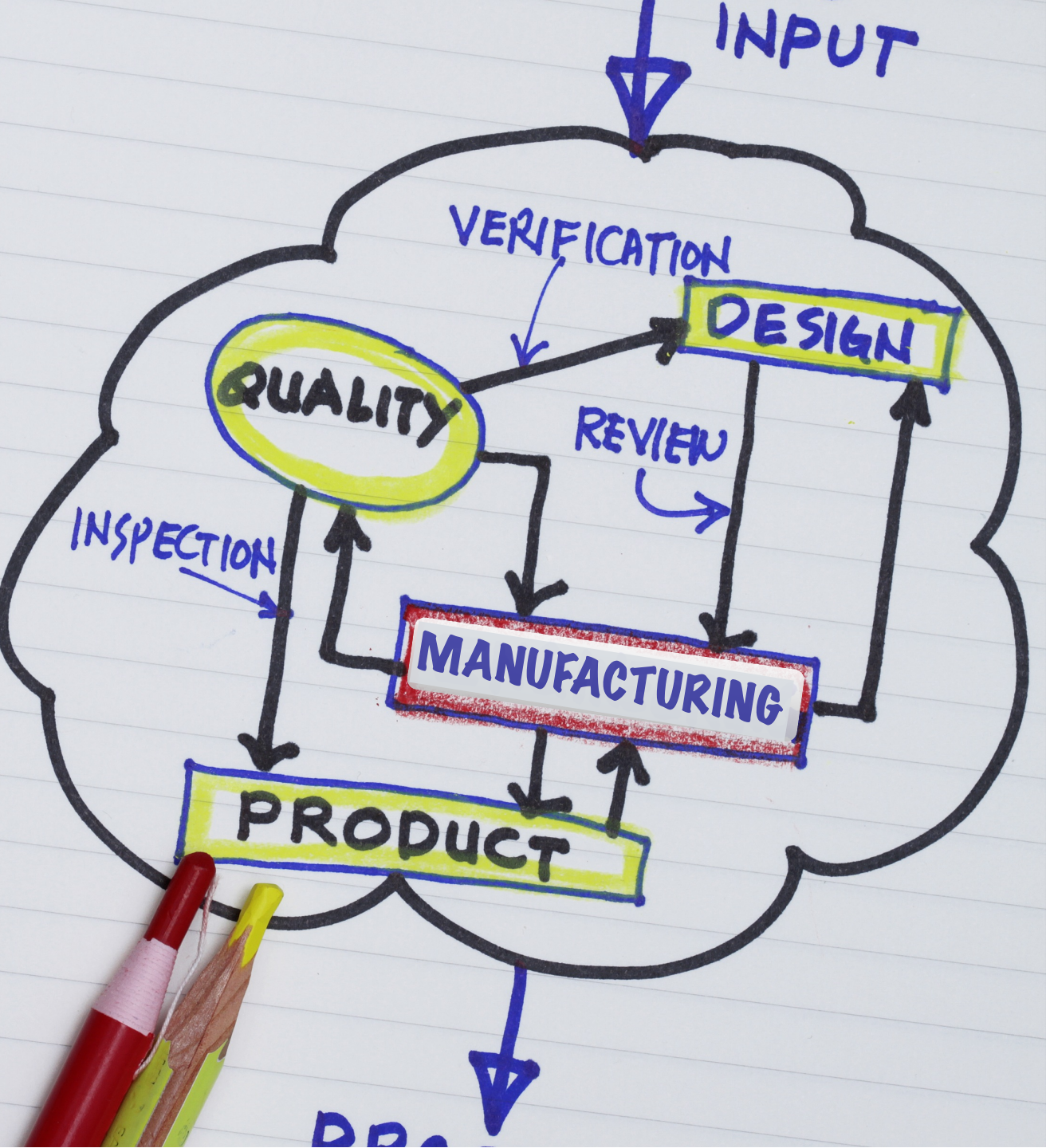

INPUT
VERIFICATION
DESIGN
QUALITY
REVIEW
INSPECTION
MANUFACTURING
PRODUCT

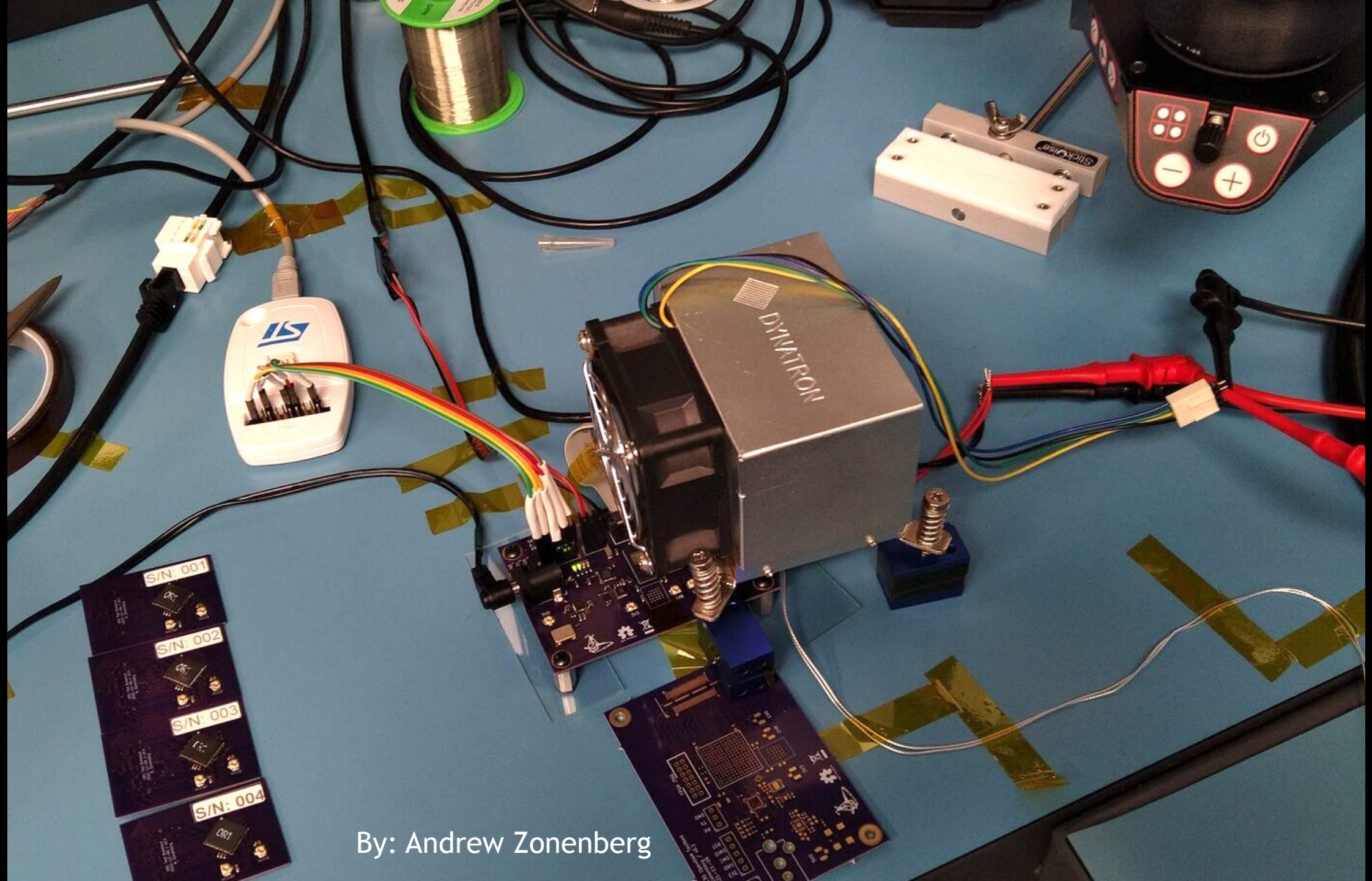
The Community
At Work

SRAM Characterization

SRAM Test Chip

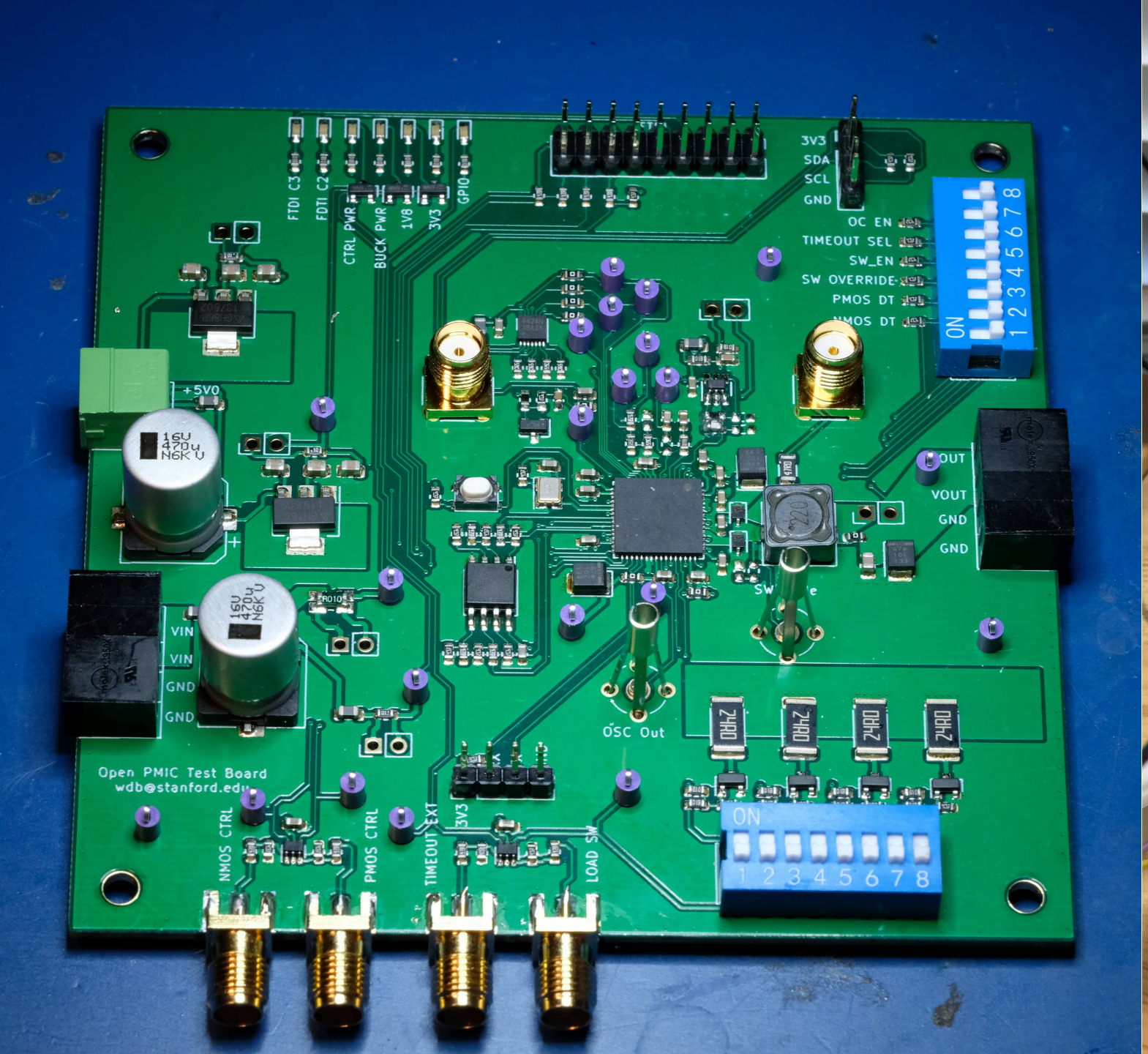
By: Andrew Zonenberg

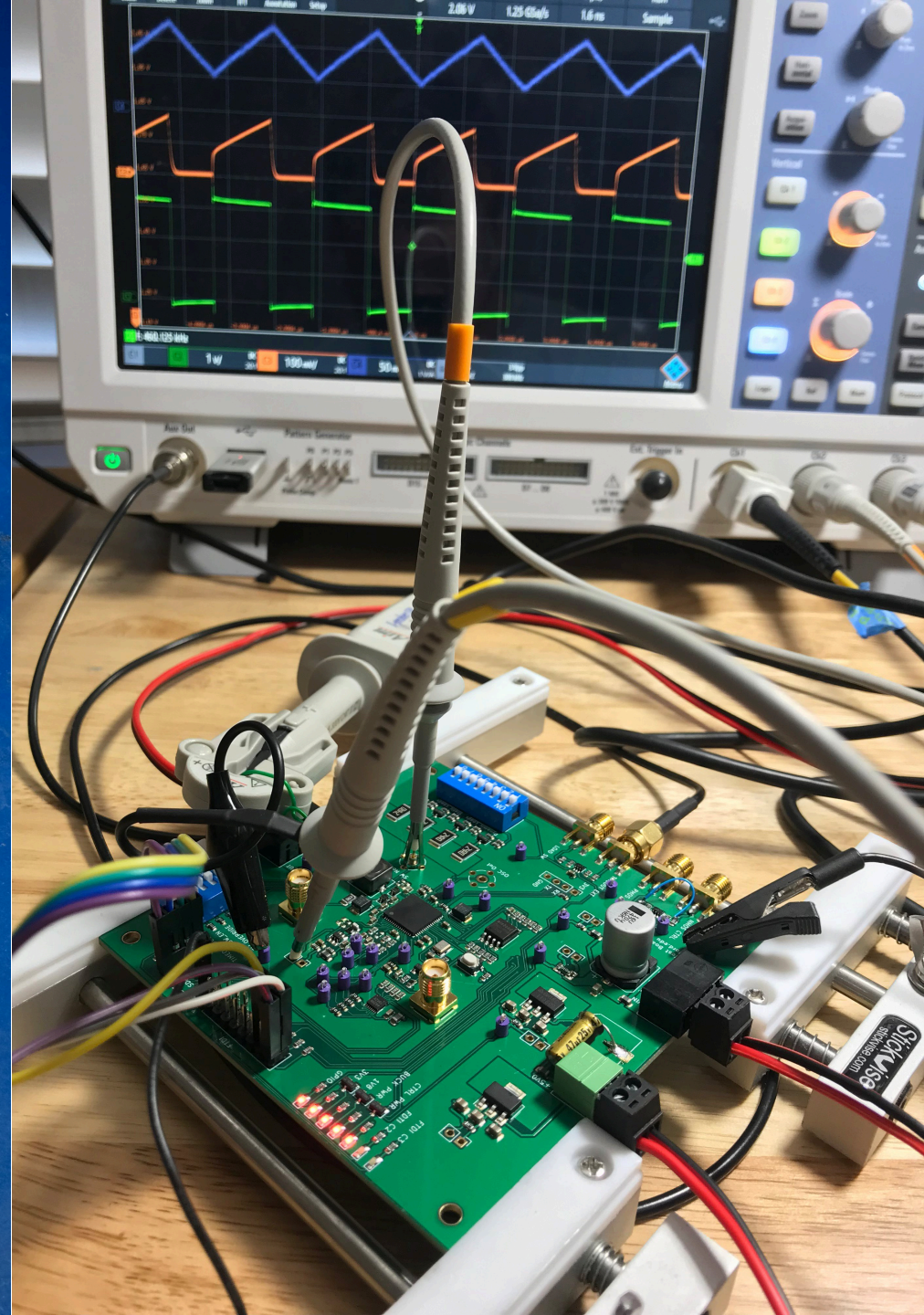
SRAM Characterization



By: Andrew Zonenberg

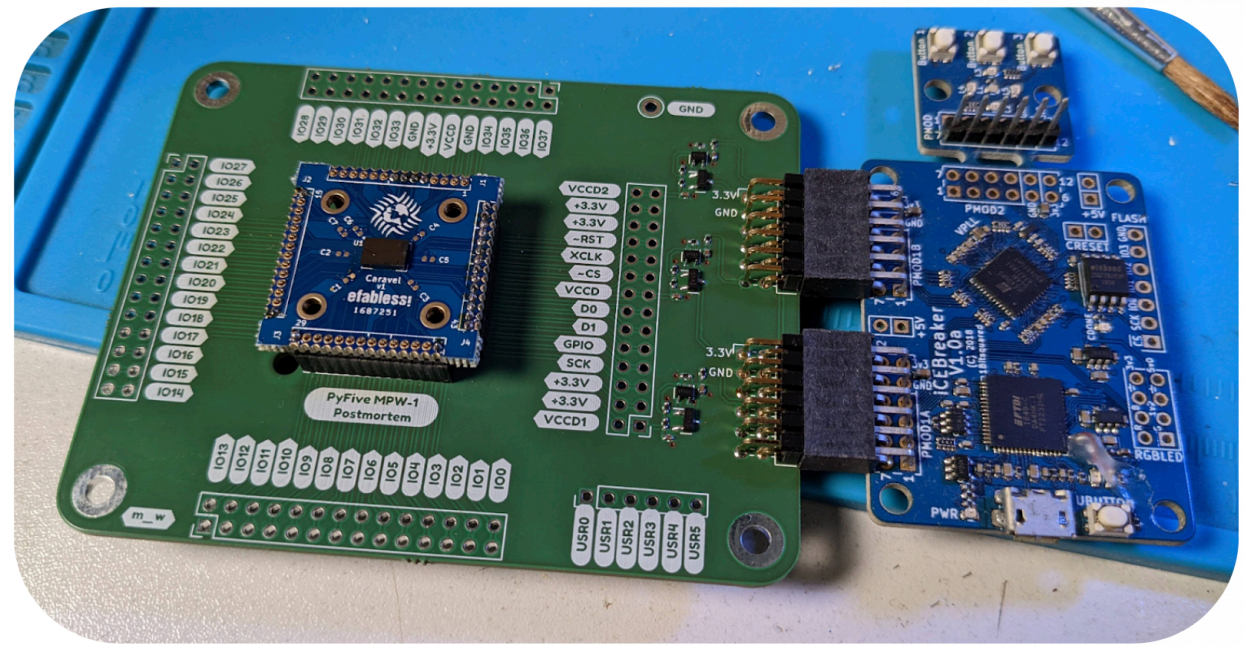
Temperature Control


FTDI C3
FDTI C2
CTRL PWR
BUCK PWR
1V8
3V3
GPIO
3V3
SDA
SCL
GND
OC EN
TIMEOUT SEL
SW_EN
SW OVERRIDE
PMOS DT
NMOS DT
ON
1 2 3 4 5 6 7 8
+5V0
16V
470u
N6K V
VIN
VIN
GND
GND
OUT
VOUT
GND
GND
OSC Out
Open PMIC Test Board
wdb@stanford.edu
NMOS CTRL
PMOS CTRL
TIMEOUT EXT
3V3
LOAD SW
ON
1 2 3 4 5 6 7 8



- www.zerotoasiccourse.com/post/mpw1-bringup/
- github.com/mattvenn/mpw1-bringup

youtu.be/f_G5ad8SbHo



bit.ly/cicc22-edu-goog

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Slide provided by: Tim Ansell

efabless.com

All my ASIC designs for Google MPW1 are working!

Zero To ASIC Course

1.1K views • 1 month ago

youtu.be/IdOvywOSSmI

bit.ly/cicc22-edu-goog

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Slide provided by: Tim Ansell

Woowzaaa!!
I'm Caravel !!

bit.ly/cicc22-edu-goog

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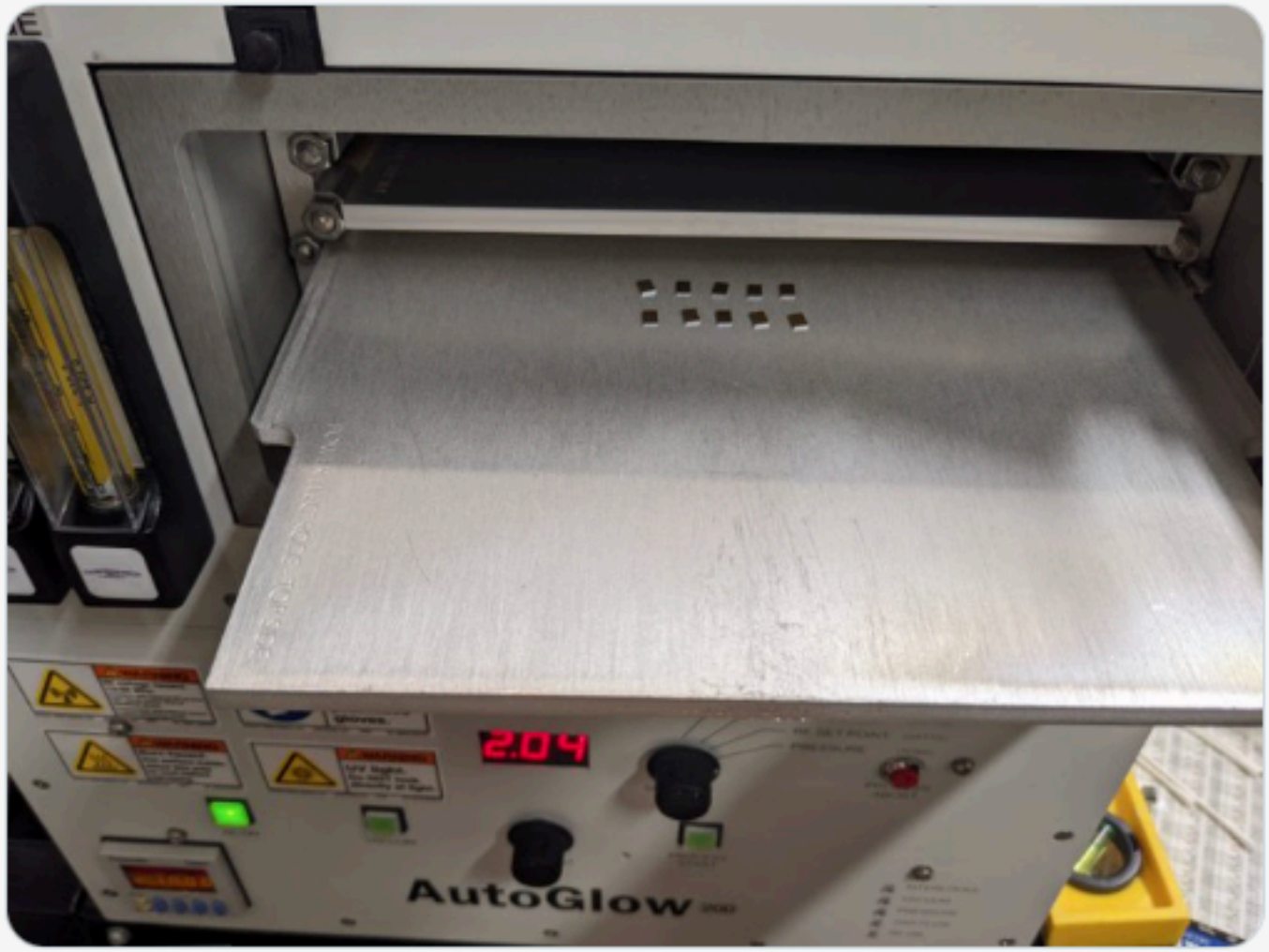
Volodymyr Pikhur @vpikhur · 15h

Replying to @vpikhur

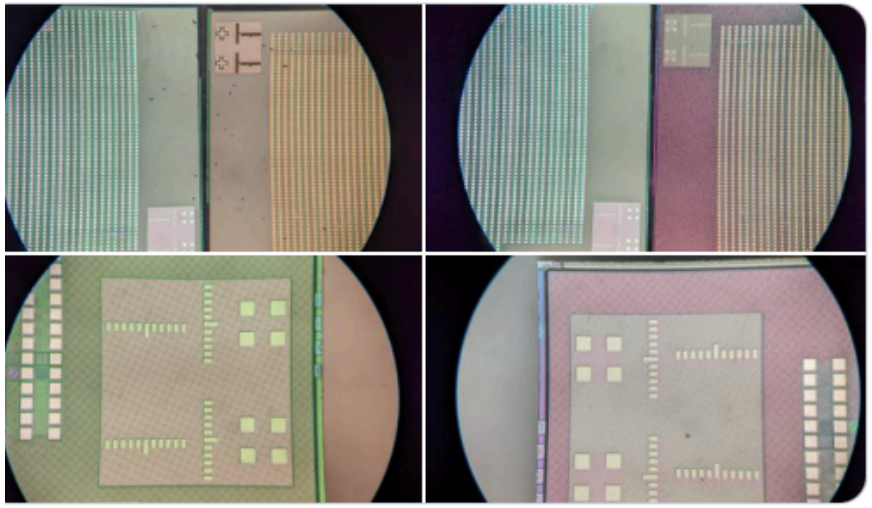
Loaded 10 samples into RIE (reactive ion etcher) to strip top polyimide layer. I use a 50/50 mix of oxygen and argon gas.



1 1 4

lodymyr Pikhur @vpikhur · 15h

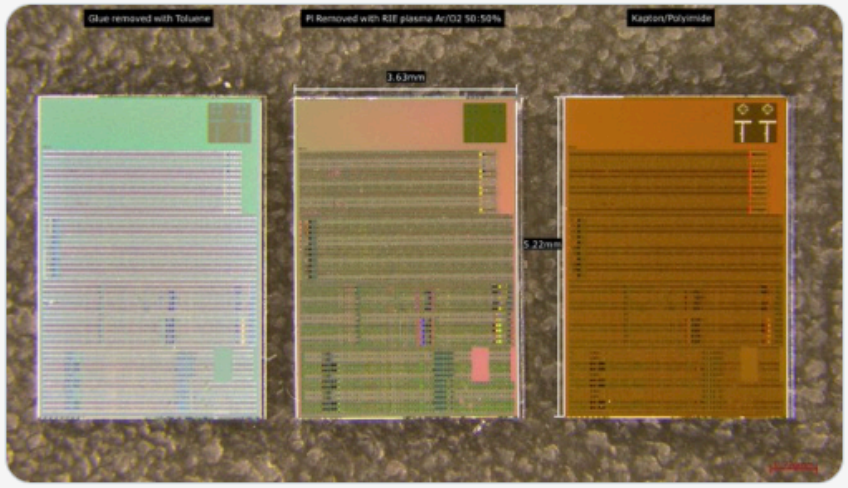
ter polyimide is removed there is adhesive/glue layer remaining. Adhesive n't be removed with normal solvents such as acetone or isopropyl cohol. Very non-polar solvent such as Toluene does the job.



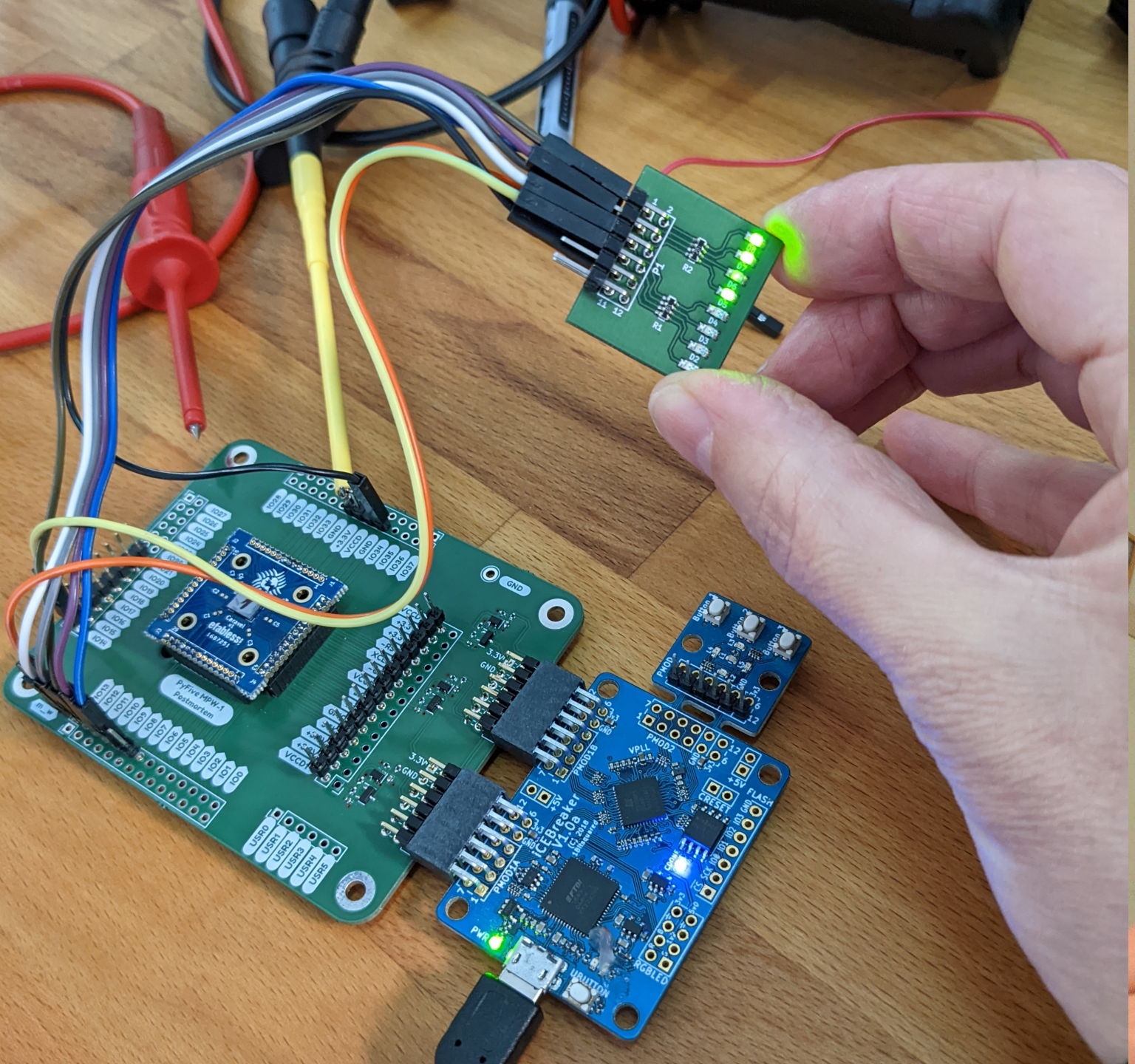
1 4 8

Volodymyr Pikhur @vpikhur · 15h

All 3 under stereo microscope with approximate die dimensions.



1 1 6


PyFive MPW-1
Postmortem
iCEBreaker
V1.0a

MPW^2

github.com/mattvenn/multi_project_tools

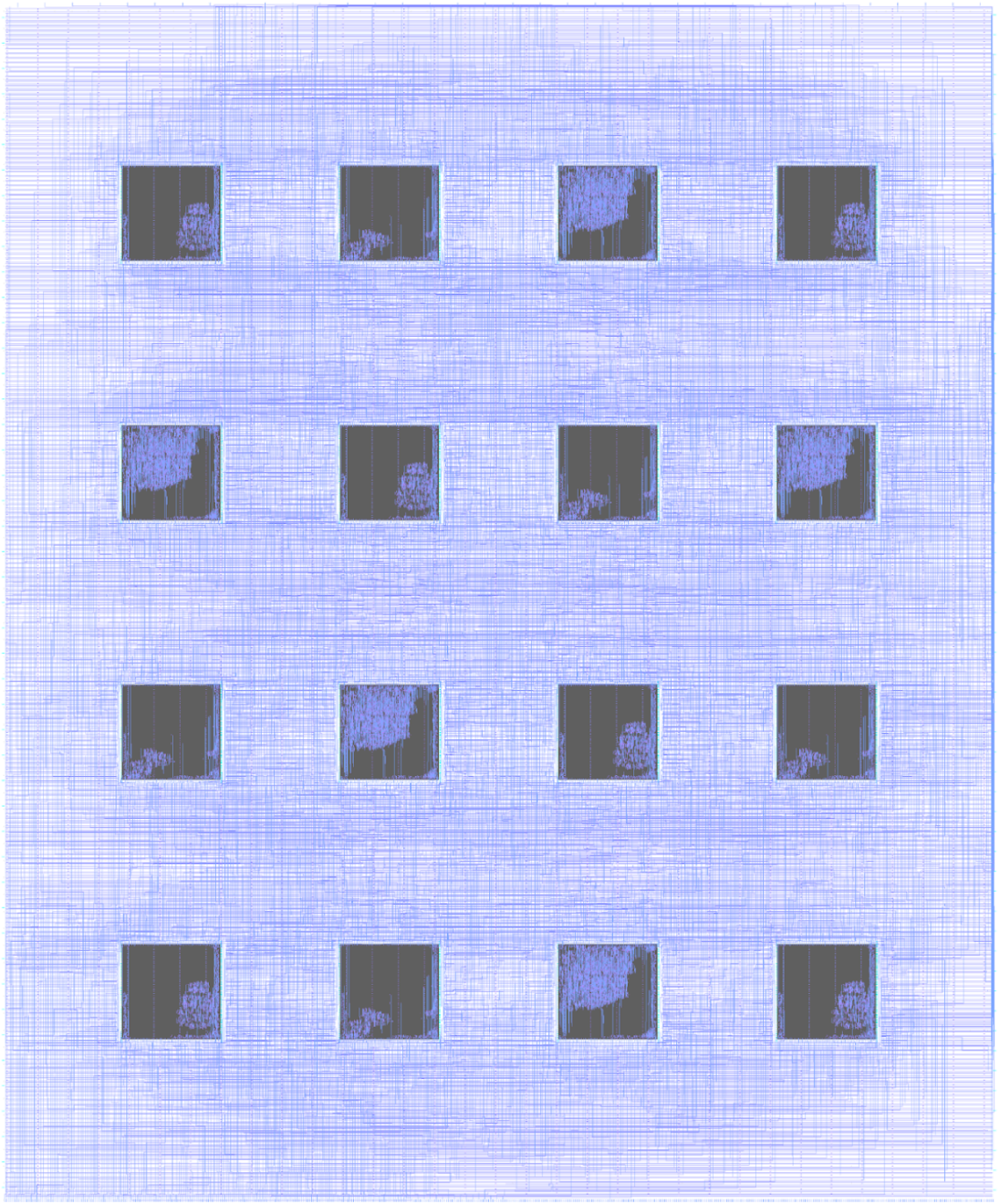
Compatible with

Open MPW *or* chipIgnite Programs

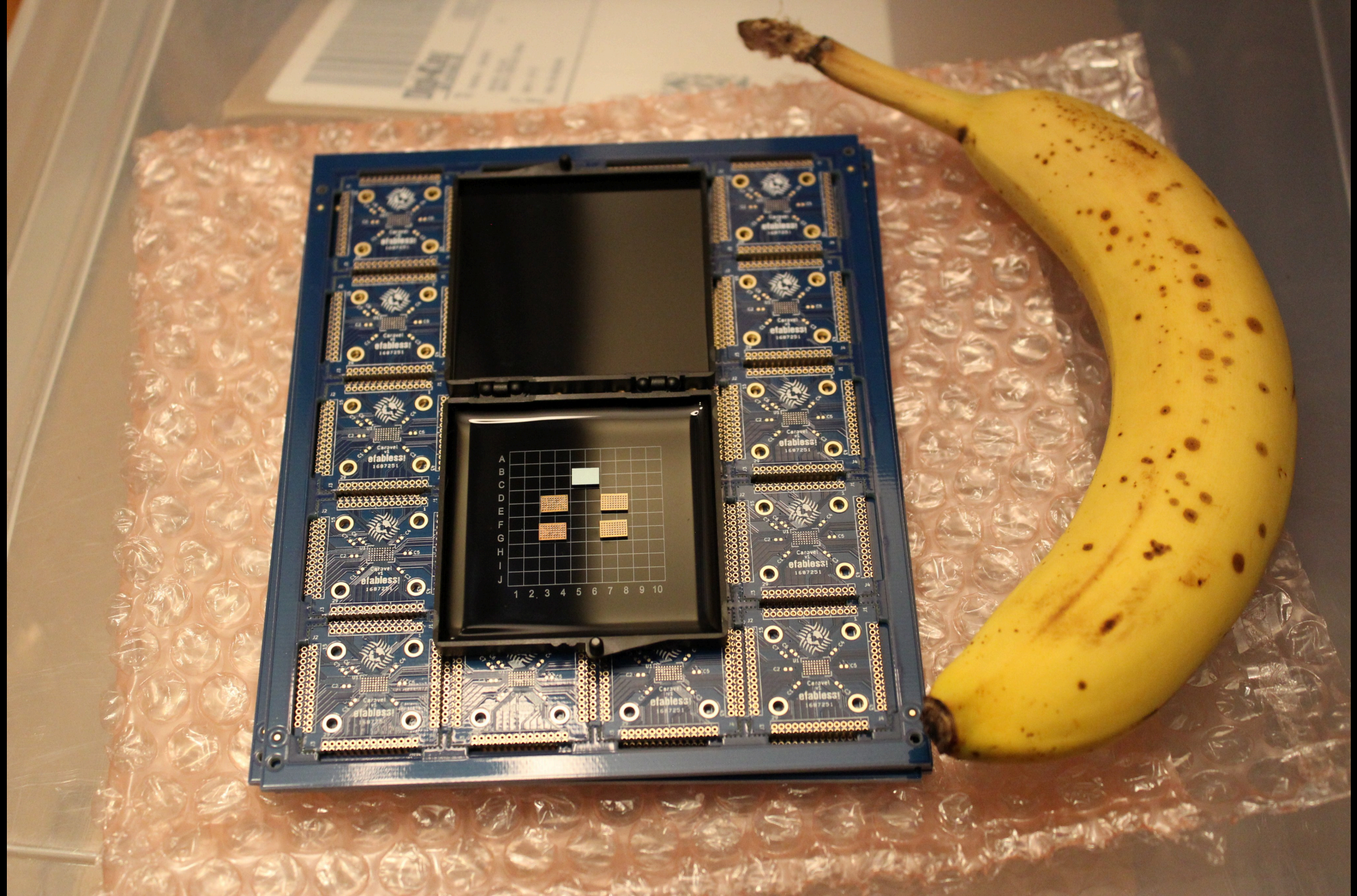
16 projects in one slot

100 ICs ÷ 16 = ~5 ICs each

$9,750 ÷ 16 = ~$610 USD



tansell@google.com


A
B
C
D
E
F
G
H
I
J
1 2 3 4 5 6 7 8 9 10
Caravel
efabless!
1607251

BUT ....

What if I do not want to open source my design?

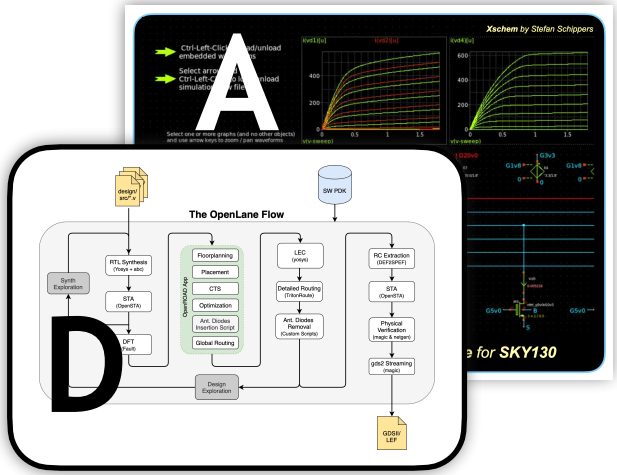
I would like to guarantee my spot on the run.

I need it on my own schedule.

chipIgnite

by efabless.com

OS EDA Digital & Analog

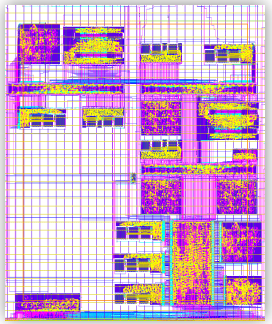


+

CARAVEL

+

User Design



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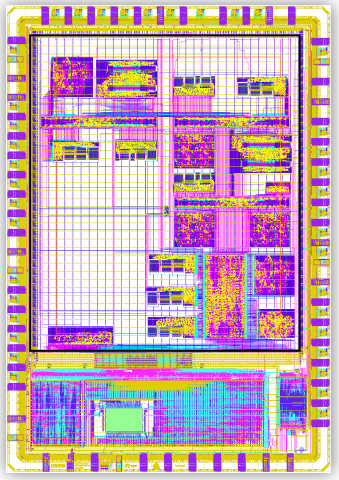


CARAVEL + User Design

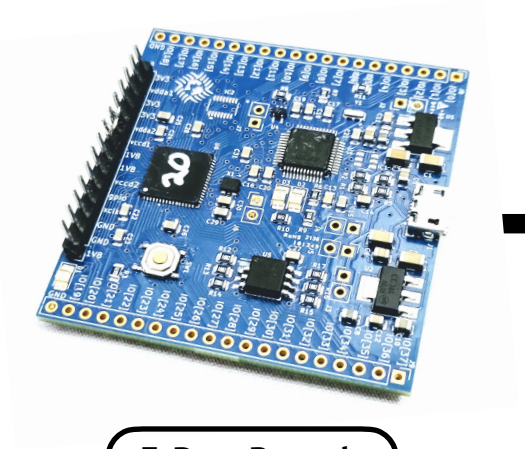
MANUFACTURING

chipIgnite

Rapid IC Creation

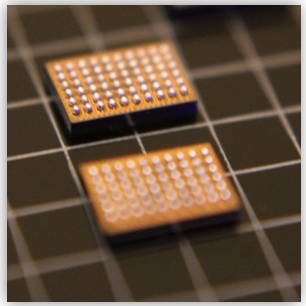
Software (FOSS)

+



5 Dev Boards

+



300 WCSP Parts

Start Here

https://ef.link/start-digital

https://ef.link/start-analog

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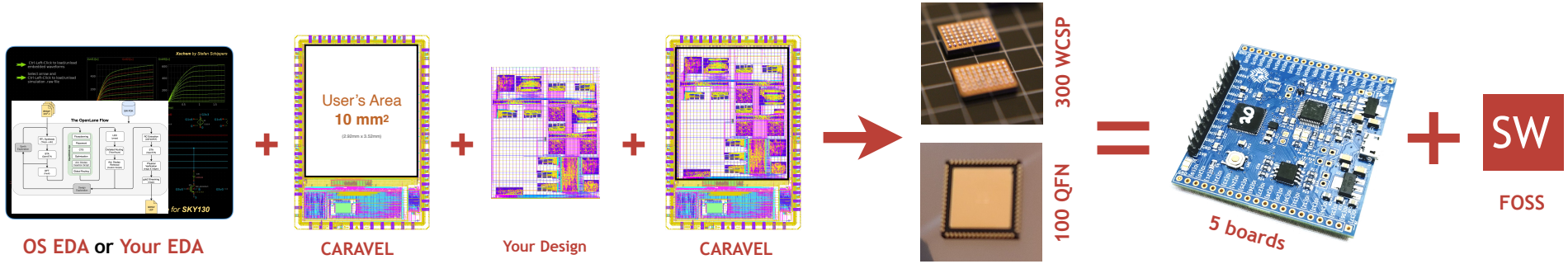
WHAT IS?

chipIgnite
Rapid IC Creation



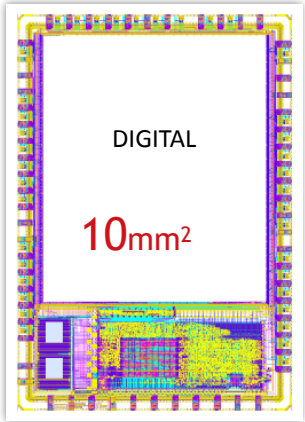
- Design using SkyWater SKY130 (130nm) rich process + std cells + IO cells
- Start from the Caravel Harness - **no cost** - book your slot for **$200**
- You *choose your licensing terms* for your design - by *default it's proprietary*
- The offered area (10mm2) is not just silicon area - *It is a framed house with plumbing and electricity - just bring your appliances*
- Cycle Time 95 days +/- depending on the package choice

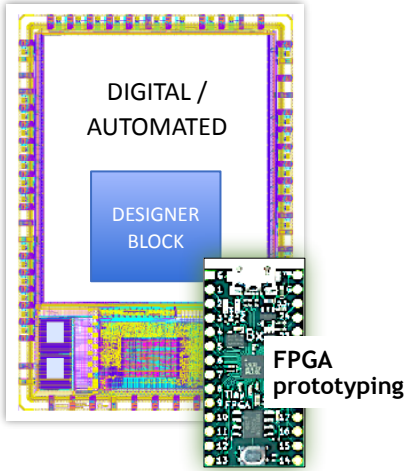
Rapid Prototyping	**$9,750**	**100 QFN**	parts + 5 dev boards
Engineering Samples	**$9,750**	**300 WCSP**	parts + 5 dev boards
Low Volume Production	**$20,000**	1000 WCSP	parts + 5 dev boards

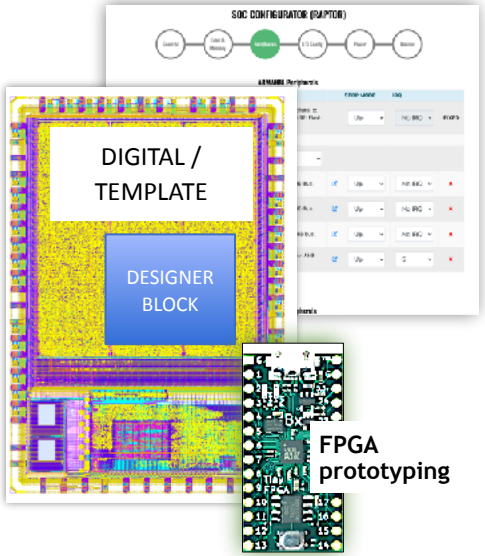
chipIgnite OPTIONS

LOW COMPLEXITY

IP Development
Digital & low frequency analog
Enabling larger designer base

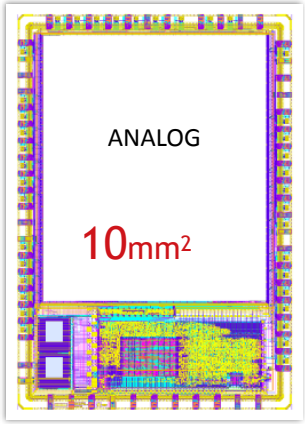


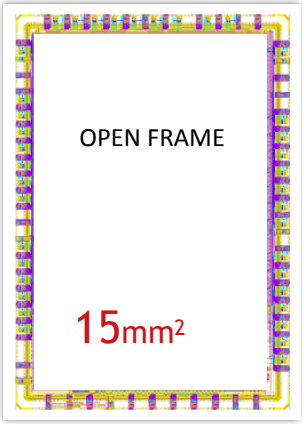


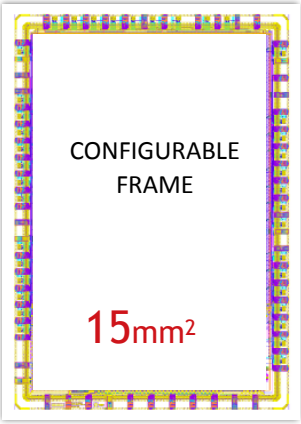


HIGH COMPLEXITY

IP Development
Complete Custom ASIC
Analog & Digital
Expert designer base







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chipIgnite CUSTOMERS

Stanford **EE272** Design Course

1

Three more universities …

High Schools coming in June 2022

IEEE SOLID-STATE CIRCUITS SOCIETY™ IC Innovation

POWERED BY chipIgnite Rapid IC Creation

SSCS "**PICO**" Open Source Design Contest:

56+ submitted designs

10 will tape out at Efabless

https://sscs.ieee.org/about/solid-state-circuits-directions/sscs-pico-program
https://efabless.com/projects/project_definition/SSCS-21

2

Open Source FPGA Foundation global program innovation among university students

3

2 **ChipIgnite** Slots per University

Turkey, Pakistan, India, Australia

4

Startups

Using chipIgnite as their proof-of-concept or low volume production

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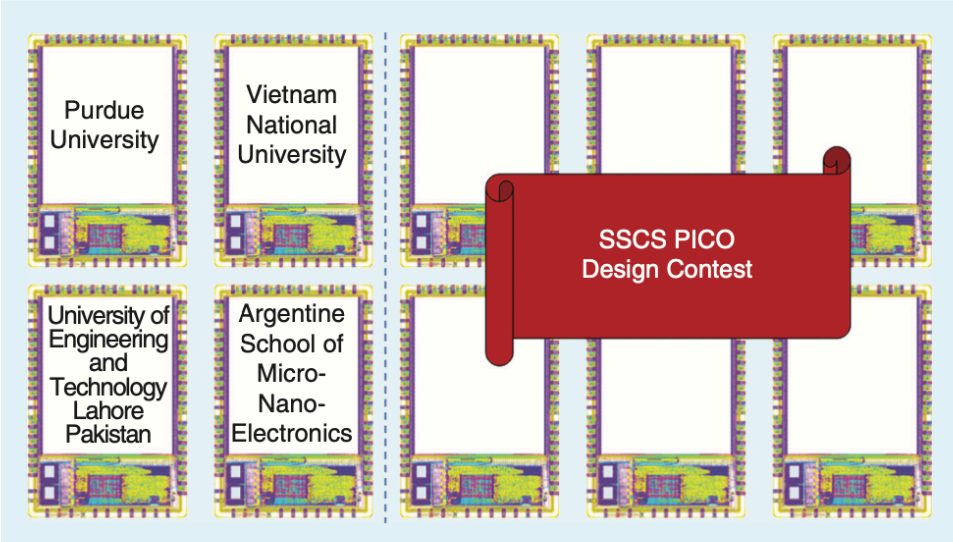
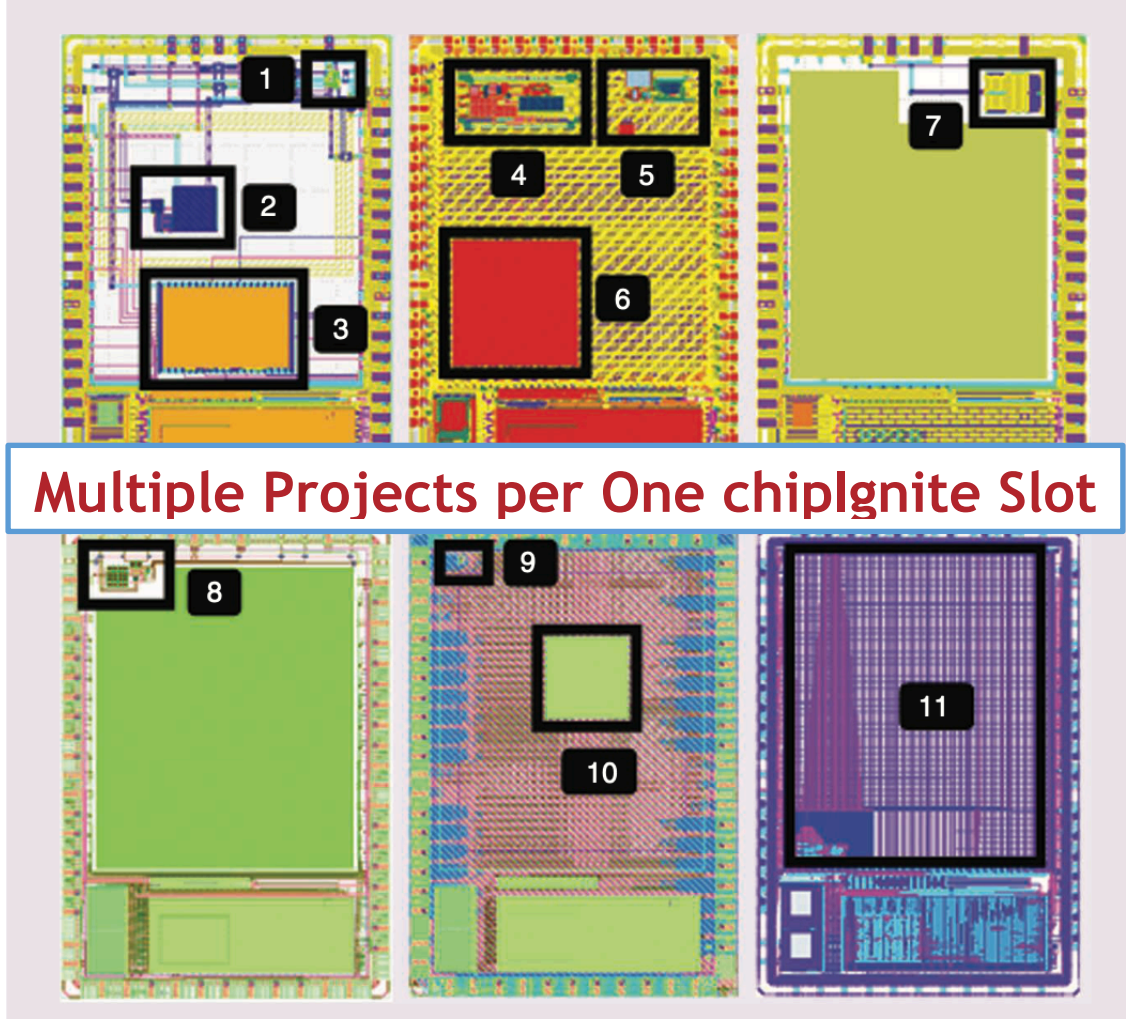
IEEE SOLID-STATE CIRCUITS SOCIETY™
IC Innovation

IEEE - PICO PROGRAM 2021

POWERED BY
chipIgnite
Rapid IC Creation



Link to Article SSCS Magazine Article - NOV 2021



Multiple Projects per One chipIgnite Slot

Link to Article SSCS Magazine Article - JAN 2022

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IEEE SOLID-STATE CIRCUITS SOCIETY™ IC Innovation

OPEN SOURCE CHIPATHON - 2022

POWERED BY chipIgnite Rapid IC Creation

Low power 130nm CMOS 10 Bit SAR ADC	https://platform.efabless.com/projects/851
Analog Baseband Circuitry For 60GHz Receivers	https://platform.efabless.com/projects/855
SPATIAL SD ADC	https://platform.efabless.com/projects/872
ENCRYPTED LSB STEGANOGRAPHY WITH AES ACCELERATOR	https://platform.efabless.com/projects/873
CMOS Bandgap Voltage Reference Design	https://platform.efabless.com/projects/874
On Chip DC-DC Converter with Fast Transient Response	https://platform.efabless.com/projects/879
DC-DC Buck Converter for efficient CubeSat EPS	https://platform.efabless.com/projects/881
CMOS Power Oscillator Test Chip	https://platform.efabless.com/projects/882
Subthreshold SRAM	https://platform.efabless.com/projects/883
Self-Interference Cancellation Low Noise Amplifier	https://platform.efabless.com/projects/888
MATRIX MULTIPLIER FOR AI ON EDGE APPLICATIONS	https://platform.efabless.com/projects/889
ReRAM based DNN accelerator	https://platform.efabless.com/projects/904
Mix-Pix - A mixed signal circuit for smart imaging	https://platform.efabless.com/projects/916
60 GHz demonstrator chip	https://platform.efabless.com/projects/920
A compact batteryless low-startup boost converter	https://platform.efabless.com/projects/922
Sub-Sampling PLL targeting SerDes Applications	https://platform.efabless.com/projects/923
Radiation-Hardened-By-Construction Microcontroller	https://platform.efabless.com/projects/928
Mixed-Signal SoC for Nanopore-Based DNA Sequencing	https://platform.efabless.com/projects/933
Digitally Enhanced PLL	https://platform.efabless.com/projects/935
Novel boost converter for battery-powered IoT uses	https://platform.efabless.com/projects/939
System on Chip for the Next Pandemic	https://platform.efabless.com/projects/945
Electrochemical Water Quality Monitoring	https://platform.efabless.com/projects/951

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chipIgnite FOR STARTUPS

Low-cost Development

Access to open-source tools enable low upfront cost for development.

Accelerated Design

Reference designs and automated design flows to enable rapid development.

You Don't Need to Be an Expert

Guided and automated flows make design easy for those without IC design experience.

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chipIgnite FOR STARTUPS

Build a PoC to support further investment

chipIgnite provides a fast low-cost path to create an initial proof-of-concept.

This can be critical to getting future investment or securing strategic customers for your startup.

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chipIgnite

for education

chipIgnite FOR CAPACITY BUILDING

open design platform makes it possible to engage **1000's of students** at any stage of education in **real life learning experience** in design, verification, prototyping and validation of **microelectronics**

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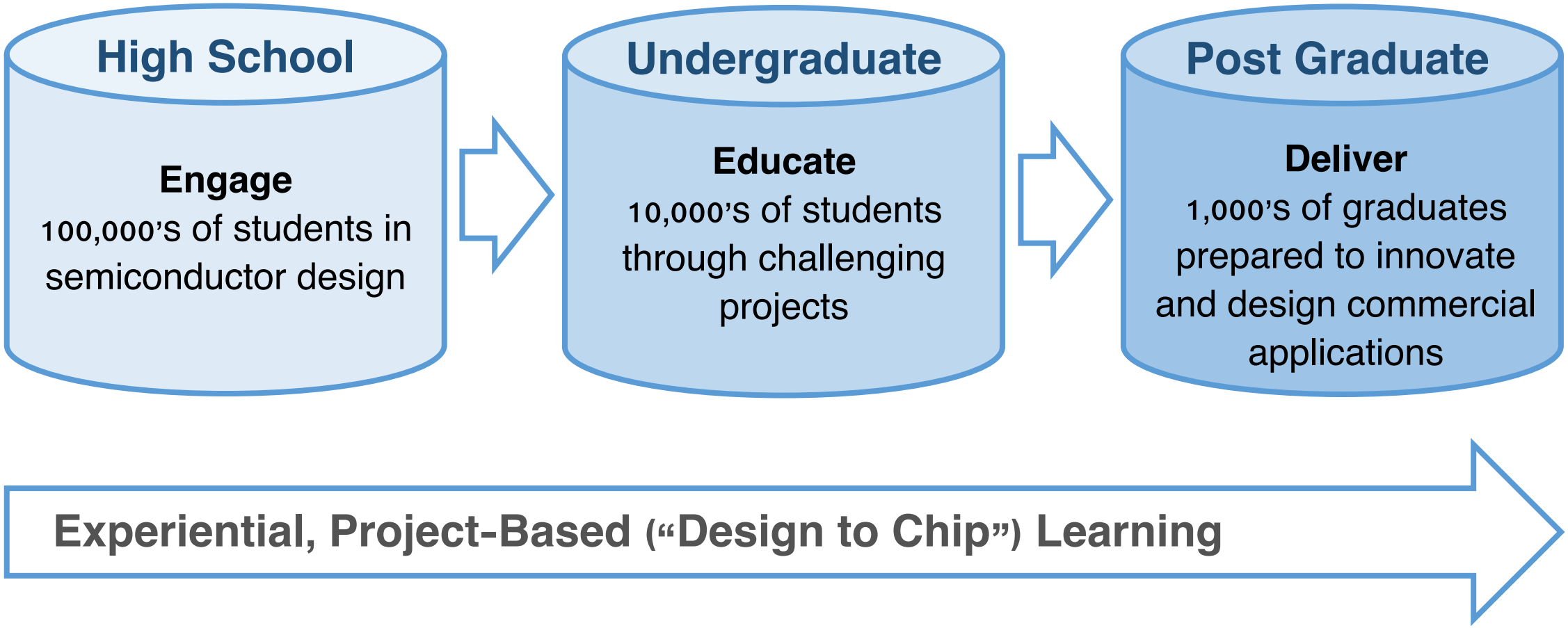
EXPERIENTIAL LEARNING AT SCALE



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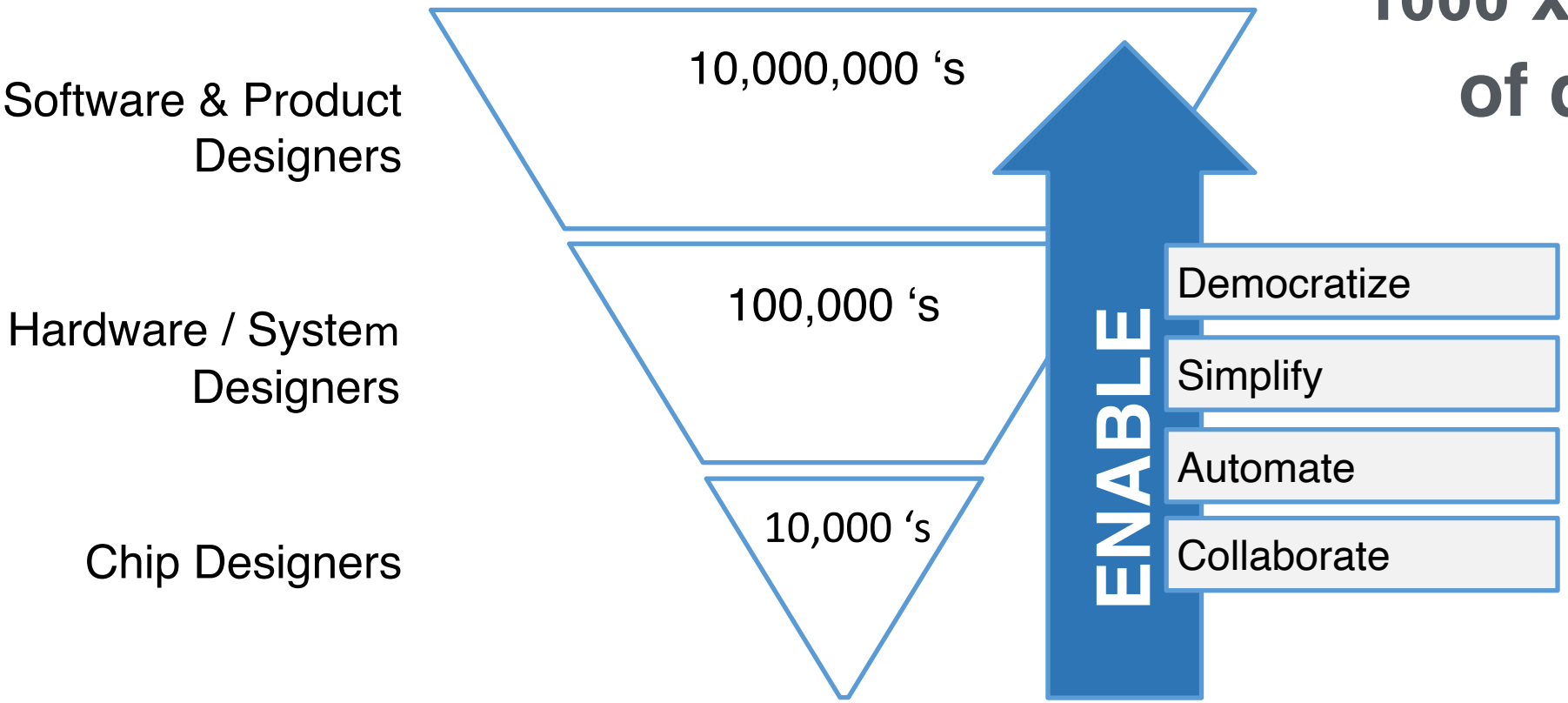
SCALING **1000X** CHIP DESIGNERS AND DESIGNS



1000 x the number of designers

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chipIgnite

FOR UNIVERSITIES

Undergraduate courses

Capstone projects

Graduate **Research**

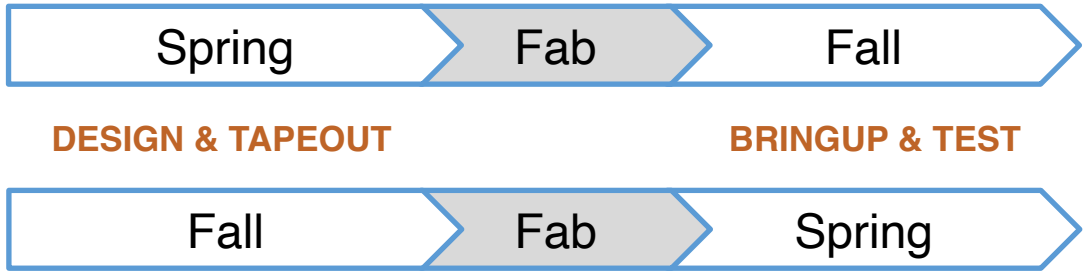
skywater

efabless.com

TAPE-OUT COURSES

Analog and / or Digital Design Courses

- **Two-session courses:**



- **Single session courses:**
  - Design + test via FPGA
  - Design + test previous student project
  - Test broken design + fix and tapeout
  - Future: one course period design/tape-out/test

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chipIgnite FOR UNIVERSITIES

Undergraduate and Graduate Courses

Provide tapeout and fabrication of student projects.

Get silicon back in the following session so students can bring-up and test their projects.

Capstone projects

Support undergraduate capstone projects with silicon fabrication.

Students can demonstrate their projects with working implementations.

Graduate research

Support graduate research and publications demonstrating results from fabricated designs.

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chipIgnite FOR UNIVERSITIES

No legal agreements

Access to the foundry technology, chip reference design, EDA tools and design flow are completely open-source.

There are no NDA or other legal agreements required. All content can be downloaded from git repos.

There are no export control restrictions, making it easy to provide access for all your domestic and international students.

Freely collaborate

No NDAs means you can freely share design files across teams and organizations, including GDS final layout files.

Collaborate with universities freely including sharing projects, course content, joint design or support design competitions.

Rapid Design

Leveraging reference designs and automated flows enables students to complete a design in a full chip within the time constraints of a single session.

Single session courses can enable students to complete a focused design goal by leveraging an existing template for a full chip.

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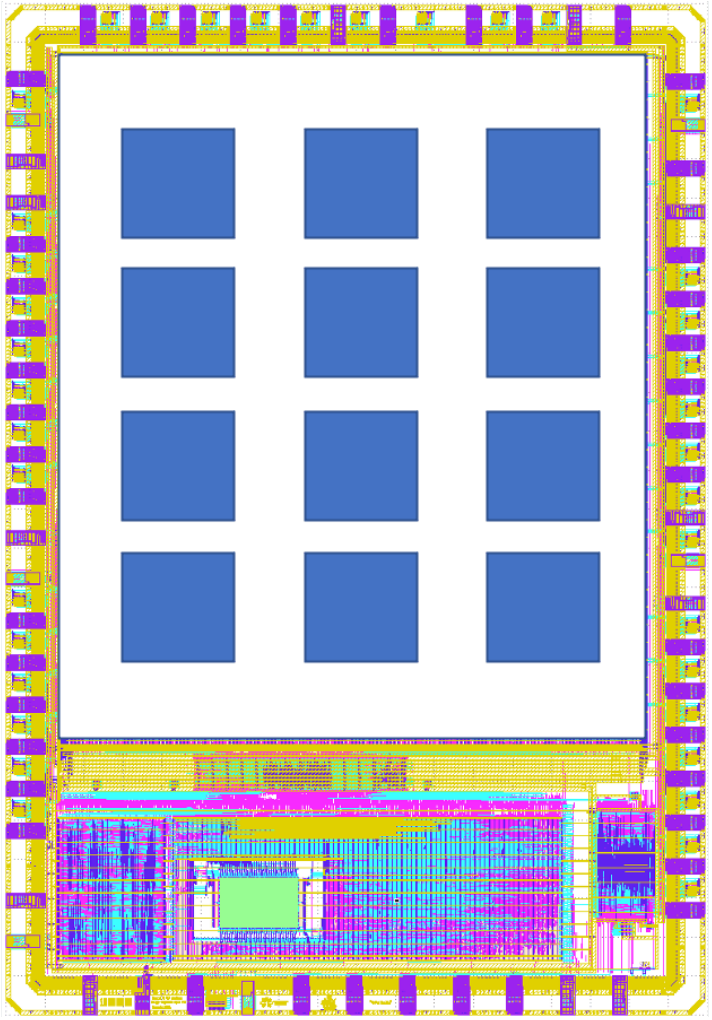
chipIgnite FOR UNIVERSITIES

Aggregate multiple projects into a single tile

Courses with smaller digital or analog student projects can be aggregated into a single project slot making fabrication very cost effective for larger class sizes.



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chipIgnite : GET STARTED

- chipIgnite Web Page
- Getting Started Video
- Project Template on Github
- Browse Previous Projects
- Join SkyWater PDK Slack Space - https://join.skywater.tools
- The OpenLane flow for digital PnR can be found at https://openlane.readthedocs.io
- The OpenROAD Project https://theopenroadproject.org/
- The documentation is at https://docs.skywater.tools
- Caravel documentation https://caravel-harness.readthedocs.io
- WOSET/ICCAD Workshop on EDA https://woset-workshop.github.io/WOSET2020.html

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GET TO SILICON

https://efabless.com

CARRIER SOC HARNESS

caravel noun

Save Word

car·a·vel | \ ˈker-ə-ˌvel, ˈka-rə-, -vəl \

Definition of *caravel*

: any of several sailing ships

A small 15th and 16th century ship that has broad bows, high narrow poop, and usually three masts with lateen or both square and later sails.

Source: https://www.merriam-webster.com/dictionary/caravel

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